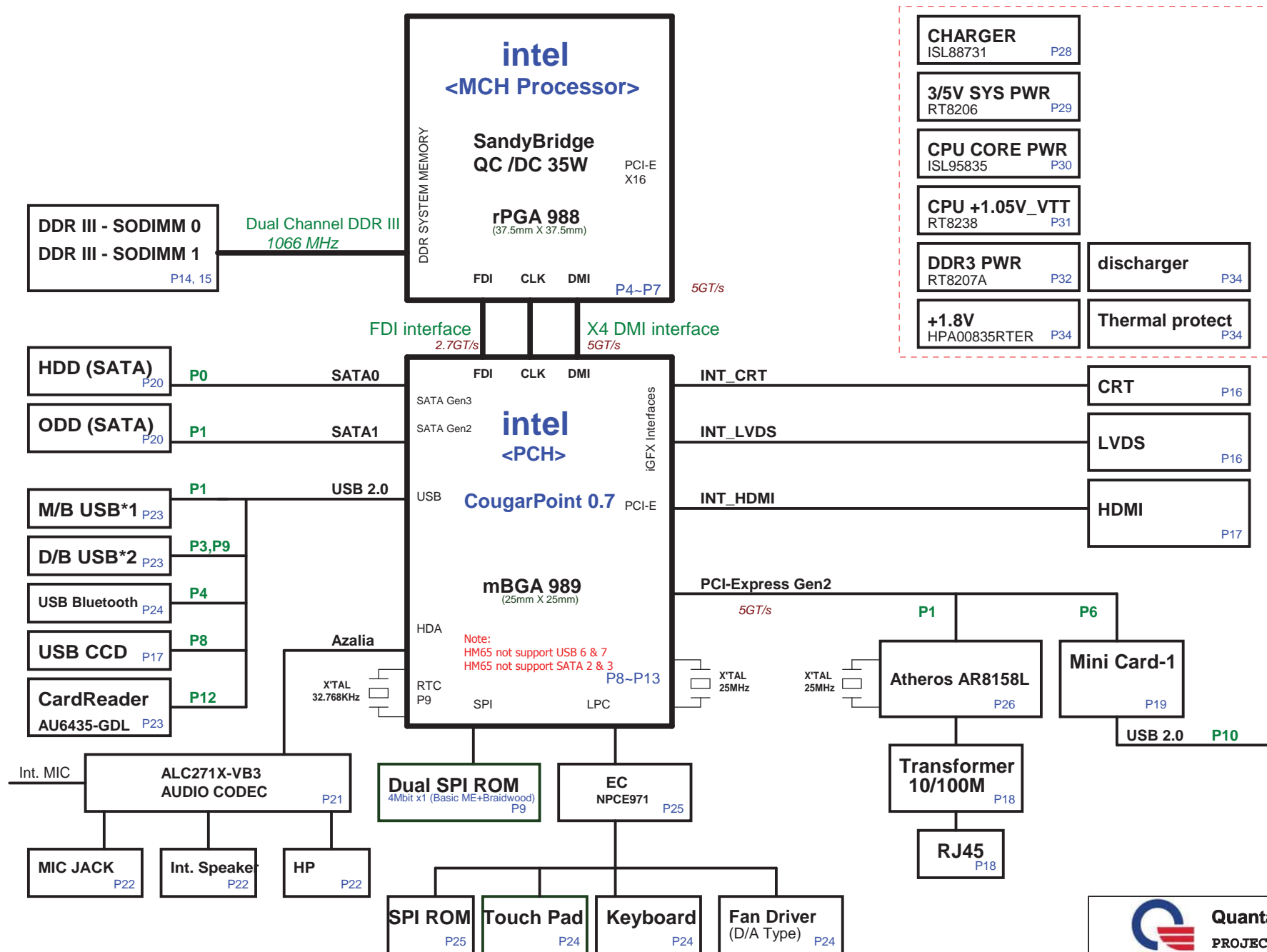


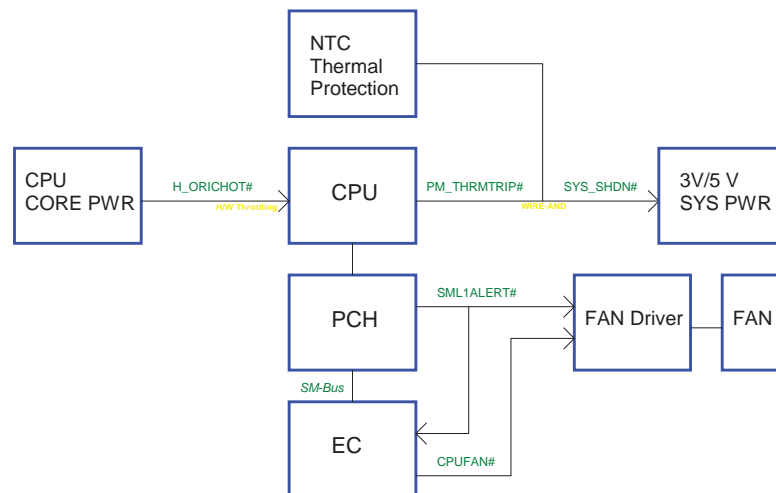
ZQR BLOCK DIAGRAM

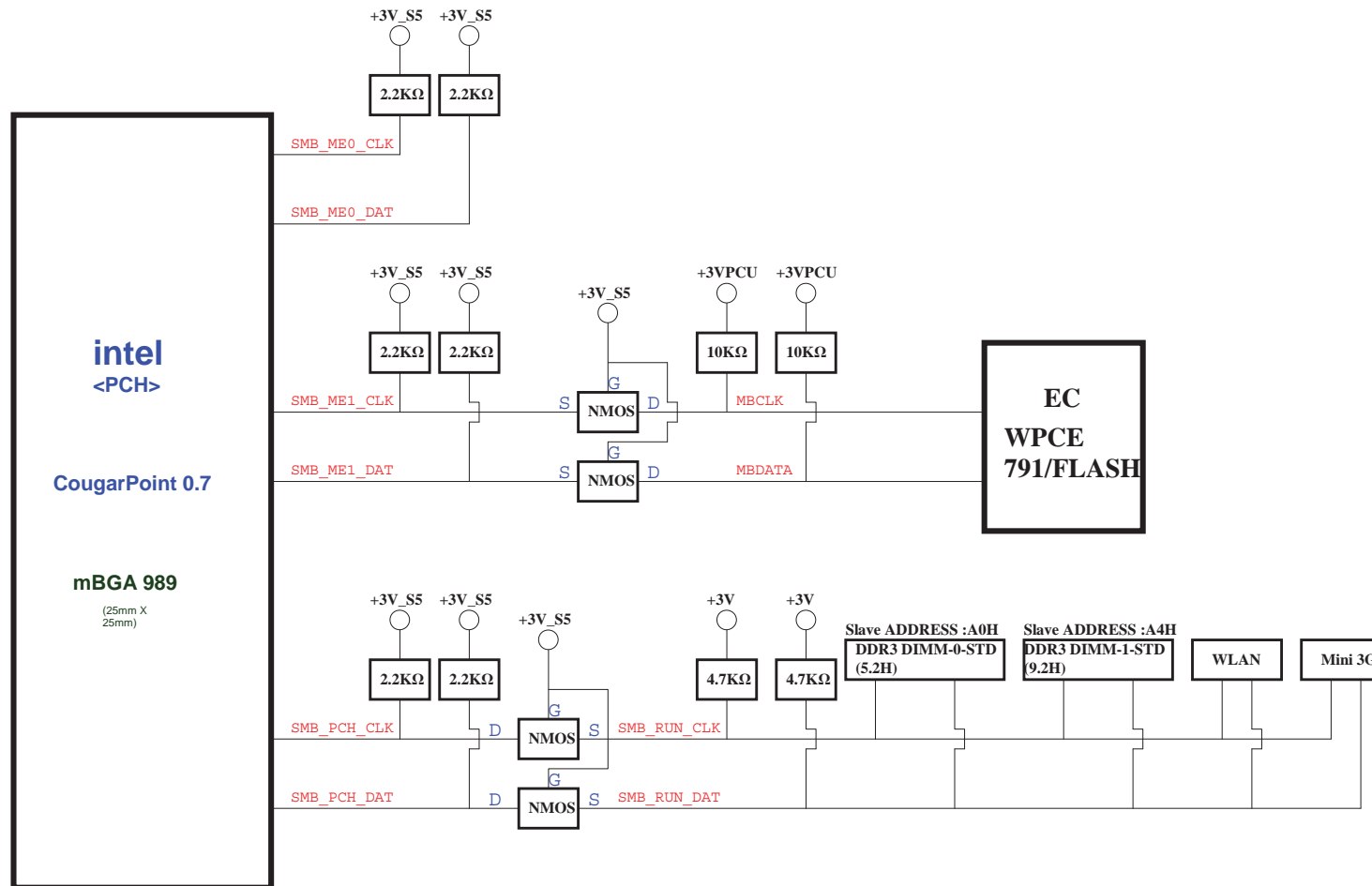


Power States

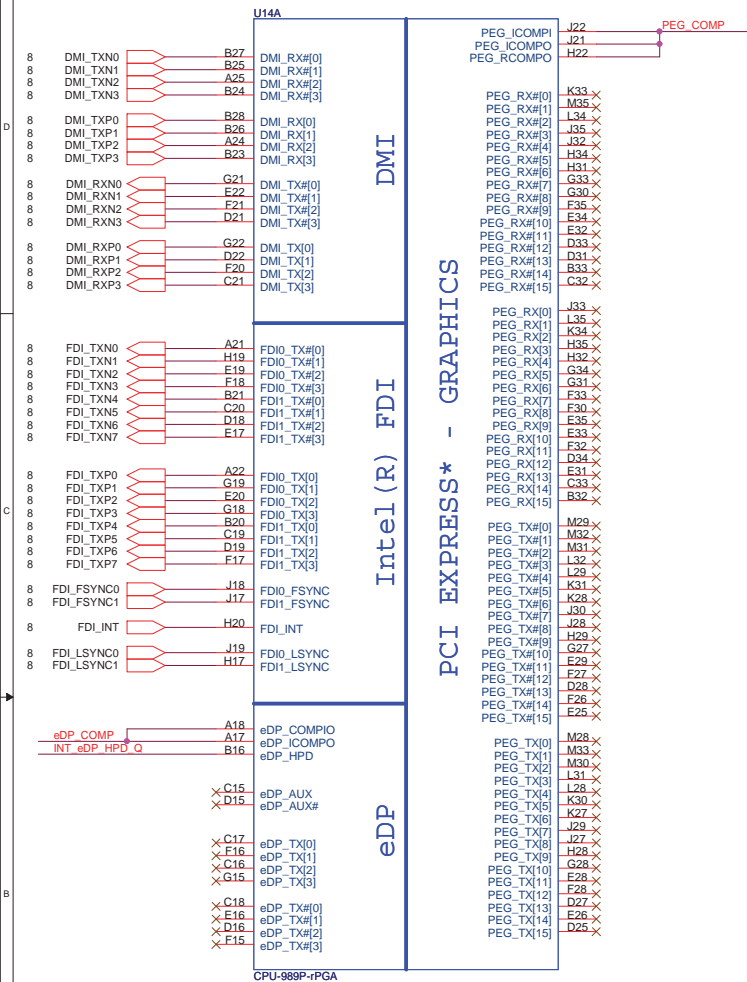
| POWER PLANE | VOLTAGE | DESCRIPTION | CONTROL SIGNAL | ACTIVE IN |
|----------------|-----------------|------------------------------------|----------------|-----------------|
| VIN | +10V~+19V | MAIN POWER | ALWAYS | ALWAYS |
| +VCCRTC | +3V~+3.3V | RTC POWER | ALWAYS | ALWAYS |
| +3VPCU | +3.3V | EC POWER | ALWAYS | ALWAYS |
| +5VPCU | +5V | CHARGE POWER | ALWAYS | ALWAYS |
| +15V | +15V | CHARGE PUMP POWER | ALWAYS | ALWAYS |
| +3V_S5 | +3.3V | LAN/BT/CIR POWER | S5_ON | S0-S5 |
| +5V_S5 | +5V | USB POWER | S5_ON | S0-S5 |
| +5V | +5V | HDD/ODD/Codec/TP/CRT/HDMI POWER | MAINON | S0 |
| +3V | +3.3V | PCH/GPU/Peripheral component POWER | MAINON | S0 |
| +1.5VSUS | +1.5V | CPU/SODIMM CORE POWER | SUSON | S0-S3 |
| +0.75V_DDR_VTT | +0.75V | SODIMM Termination POWER | MAINON | S0 |
| +VGFX_AXG | variation | Internal GPU POWER | GFX_ON | S0 |
| +1.8V | +1.8V | CPU/PCH/Braidwood POWER | MAINON | S0 |
| +1.5V | +1.5V | MINI CARD/NEW CARD POWER | MAINON | S0 |
| +1.1V_VTT | +1.05V or +1.1V | CPU VTT POWER | MAINON | S0 |
| +1.05V | +1.05V | PCH CORE POWER | MAINON | S0 |
| +VCC_CORE | variation | CPU CORE POWER | VRON | S0 |
| LCDVCC | +3.3V | LCD POWER | LVDS_VDDEN | S0 |
| +5V_GPU | +5V | SWITCHABLE PWM IC POWER | dGPU_PWR_EN# | Discrete enable |
| +GPU_CORE | +0.9V~+1.1V | GPU CORE POWER | +3V_D | Discrete enable |
| +GPU_IO | +0.9V~+1.1V | GPU I/O POWER | PG_GPUIO_EN | Discrete enable |
| +1.5V_GPU | +1.5V | VRAM CORE POWER | PG_1.5V_EN | Discrete enable |
| +1.8V_GPU | +1.8V | GPU_CRE/LVDS/PLL POWER | +1.5V_GPU | Discrete enable |
| +1V | +1V | DP/PEG POWER | PG_1V_EN | Discrete enable |

Thermal Follow Chart



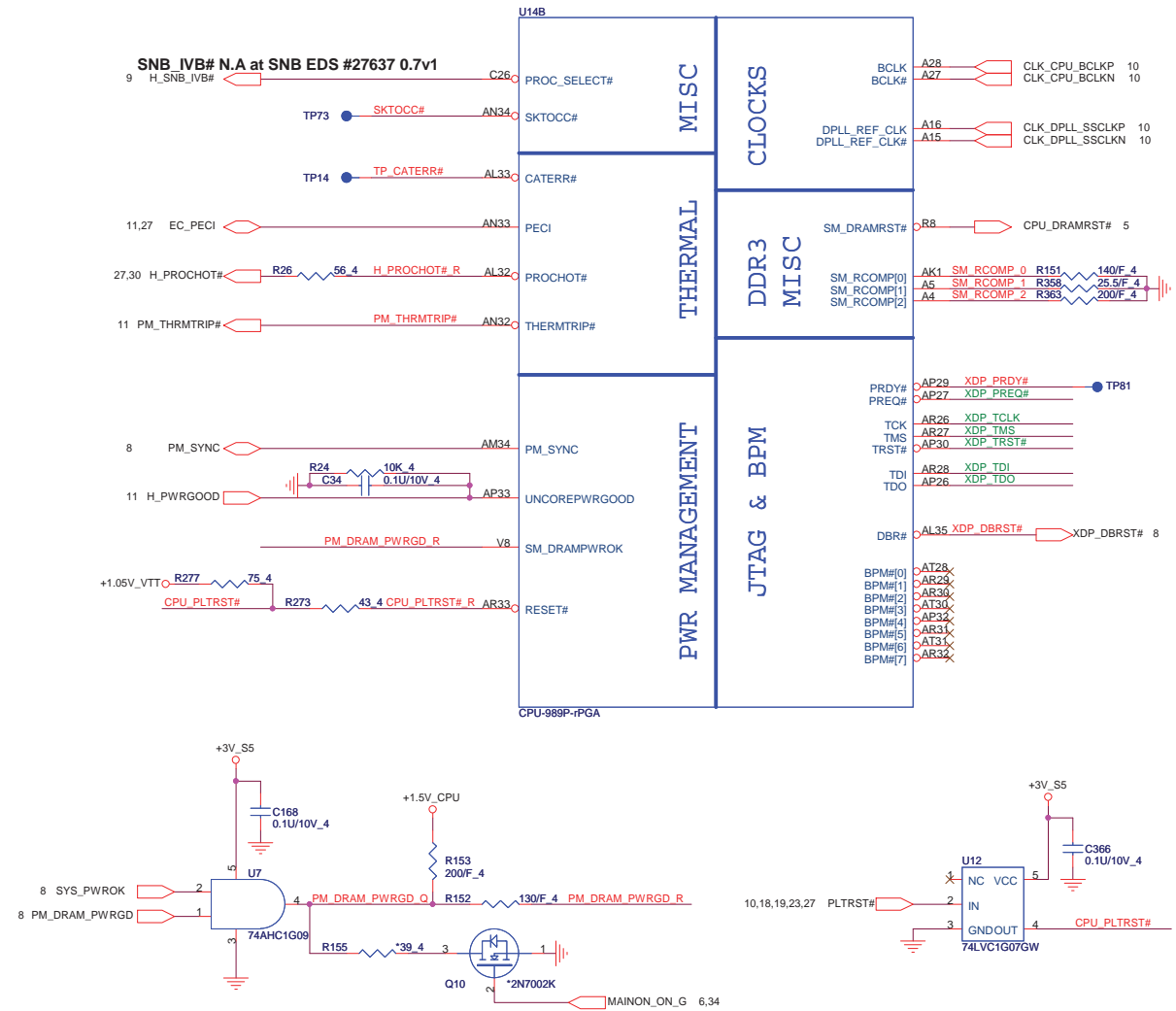


Sandy Bridge Processor (DMI,PEG,FDI)

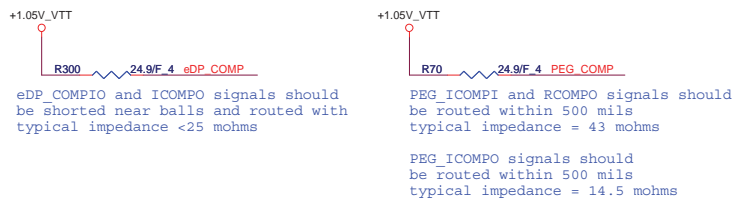


Sandy Bridge Processor (CLK,MISC,JTAG)

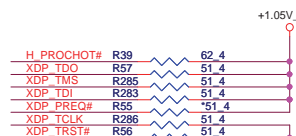
04



DP & PEG Compensation



Processor pull-up(CPU)



<http://hobi-elektronika.net>

eDP Hot-plug

HPD disable

INT_eDP_HPDI_Q

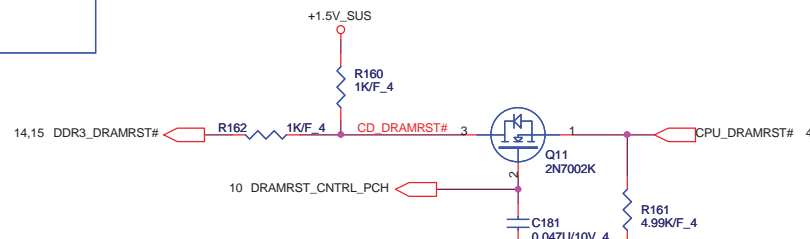


Quanta Computer Inc.

PROJECT : ZQR

| Size | Document Number | Rev |
|----------------------------|------------------|-----|
| | Sandy Bridge 1/4 | 1A |
| Date: Monday, May 23, 2011 | Sheet 4 of 35 | |

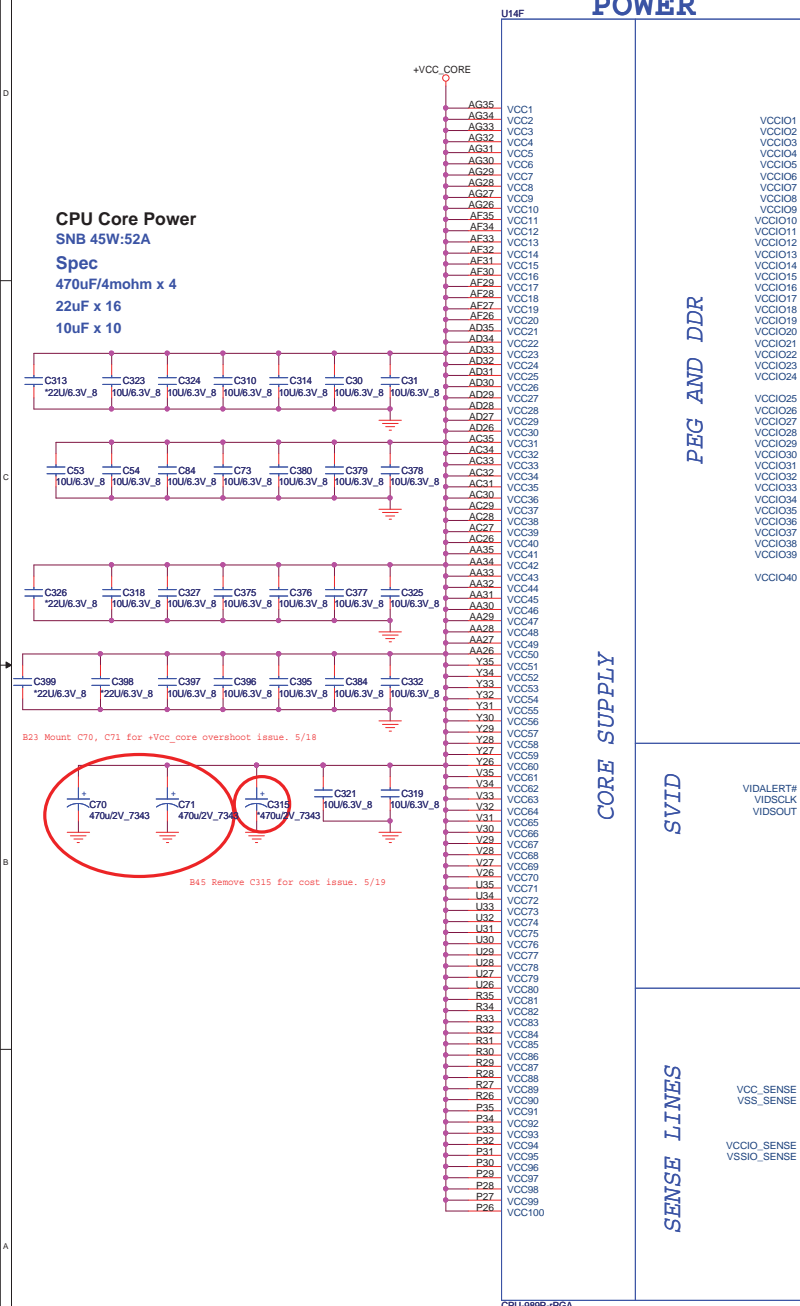
05



POWER

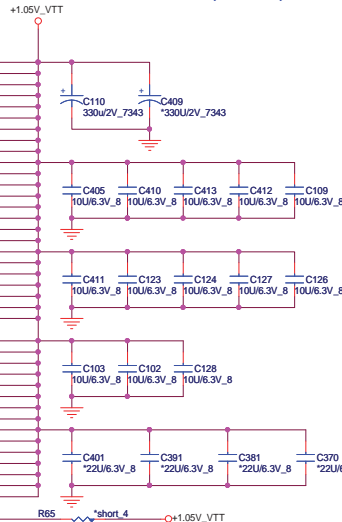
CPU Core Power
SNB 45W:52A

Spec
470uF/4mohm x 4
22uF x 16
10uF x 10



SNB 45W:8.5A

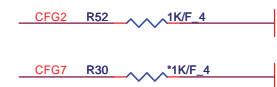
Spec
330uF/6mohm x 2
22uF x 12
22uF x 7 (Non-stuff)



07



| | 1 | 0 |
|------------------------------------|--|--|
| CFG2 (PEG Static Lane Reversal) | Normal Operation | Lane Reversed |
| CFG4 (DP Presence Strap) | Disable; No physical DP attached to eDP | Enable; An ext DP device is connected to eDP |
| CFG7 (PEG Defer Training) | PEG train immediately following xxRESETB de assertion | PEG wait for BIOS training |



```
11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled
```

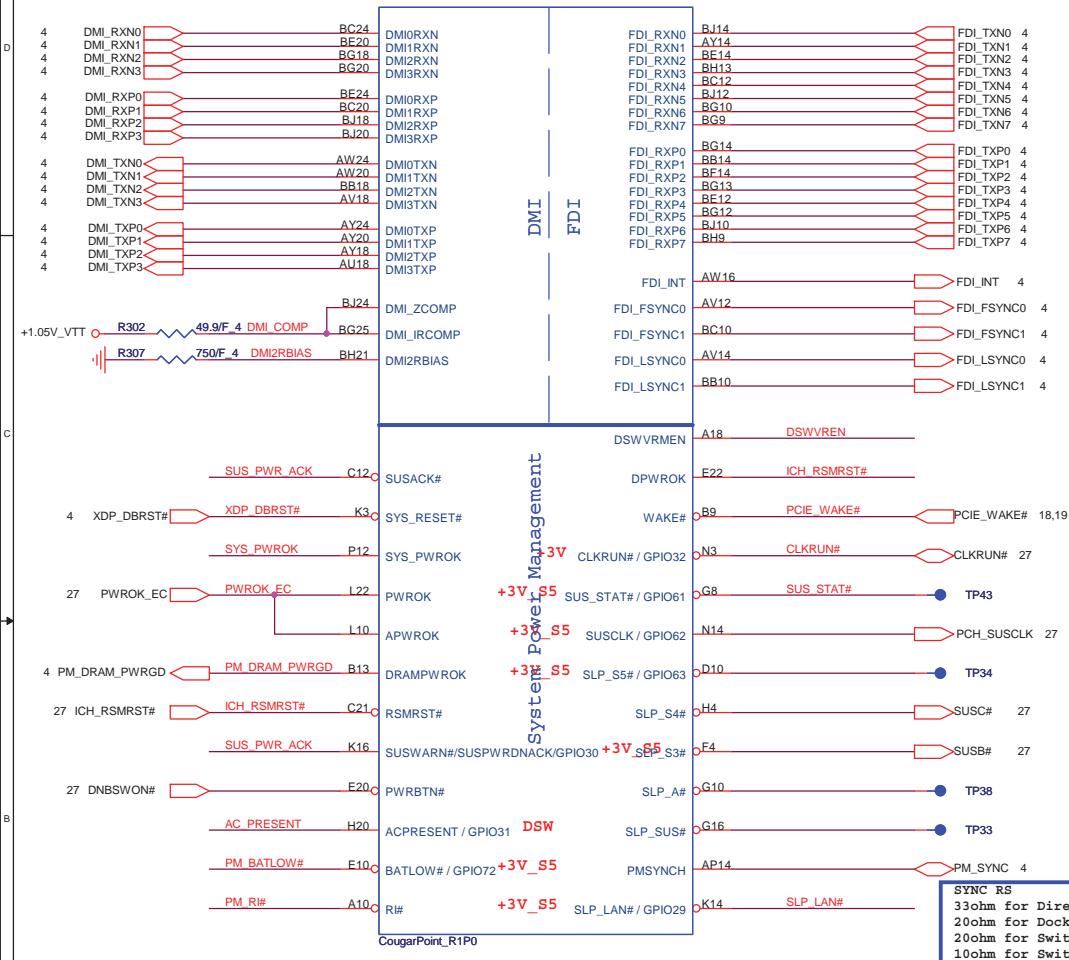


PROJECT : ZQR

| | | |
|-------|-------------------------|---------------|
| Size | Document Number | Rev |
| | Sandy Bridge 4/4 | 1A |
| Date: | Monday, May 09, 2011 | Sheet 7 of 35 |

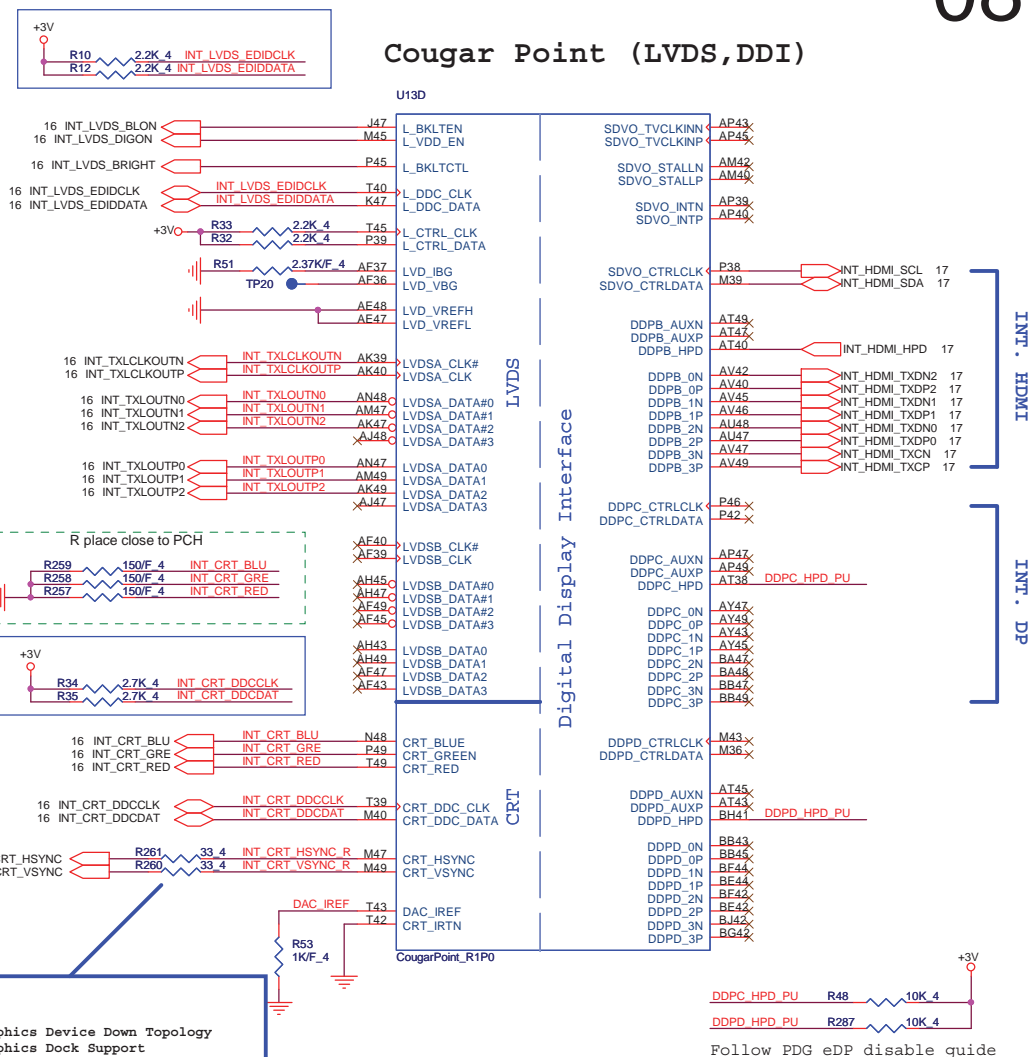
Cougar Point (DMI, FDI, PM)

U13C

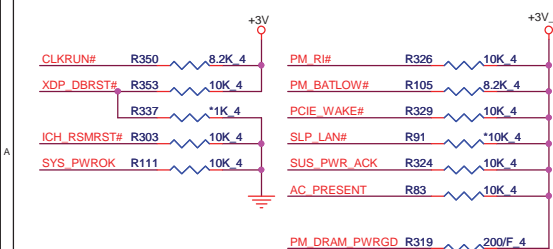


Cougar Point (LVDS, DDI)

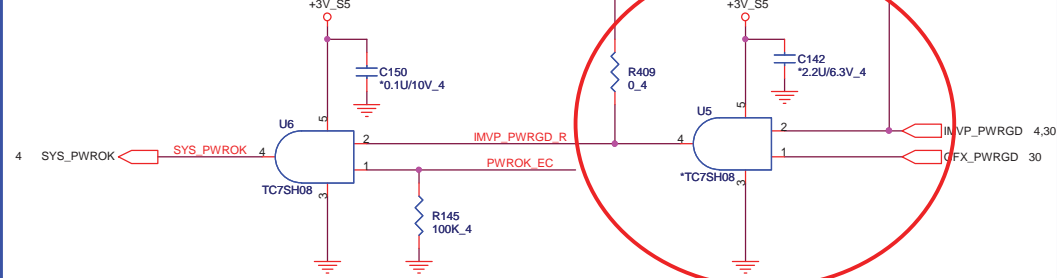
U13D



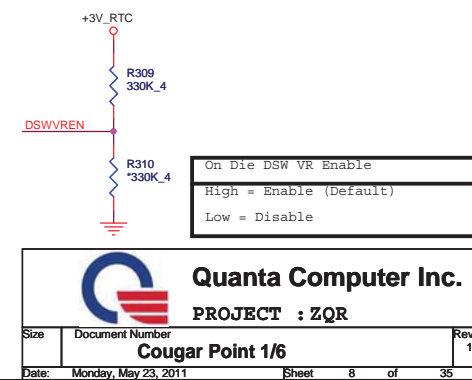
PCH Pull-high/low(CLG)



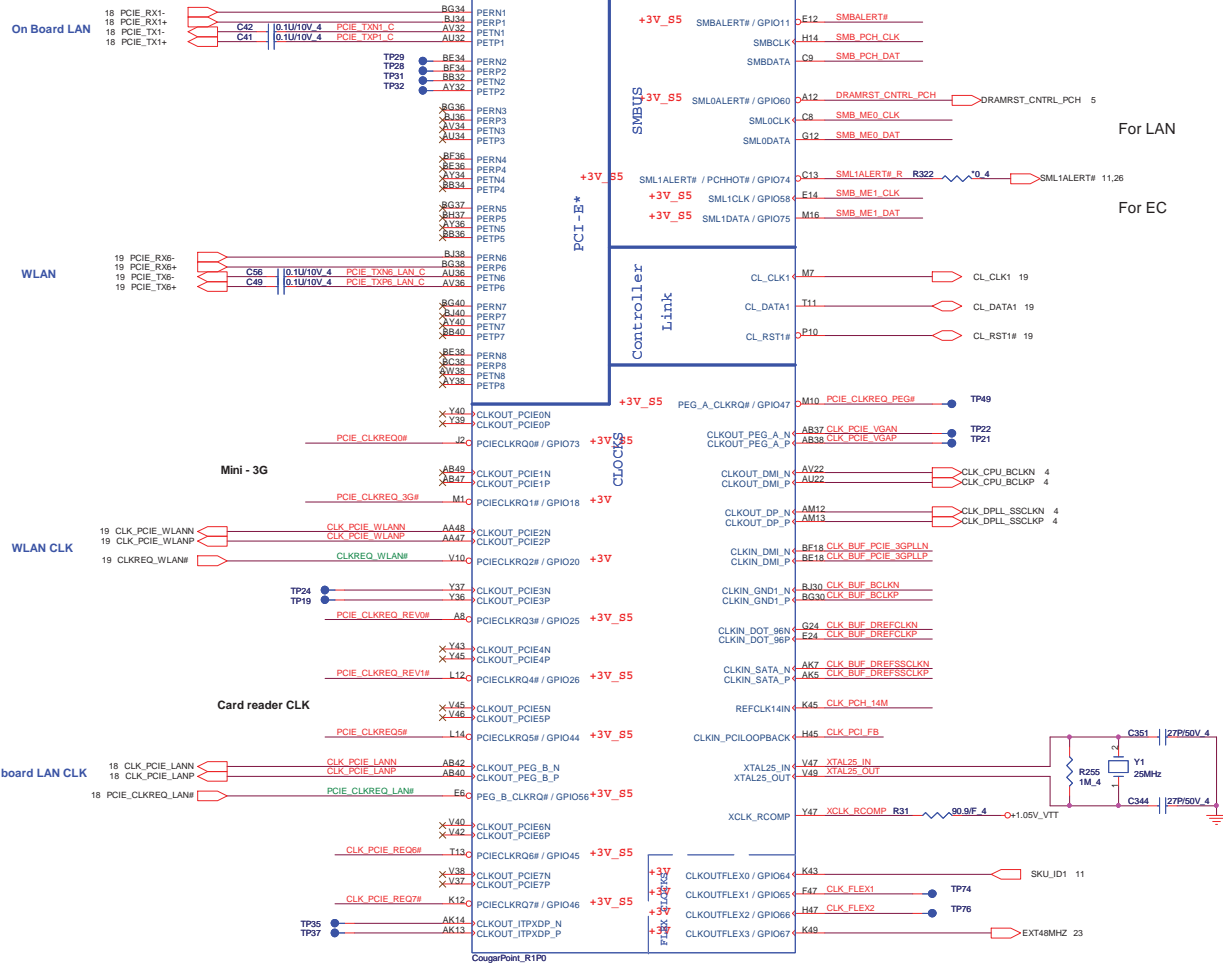
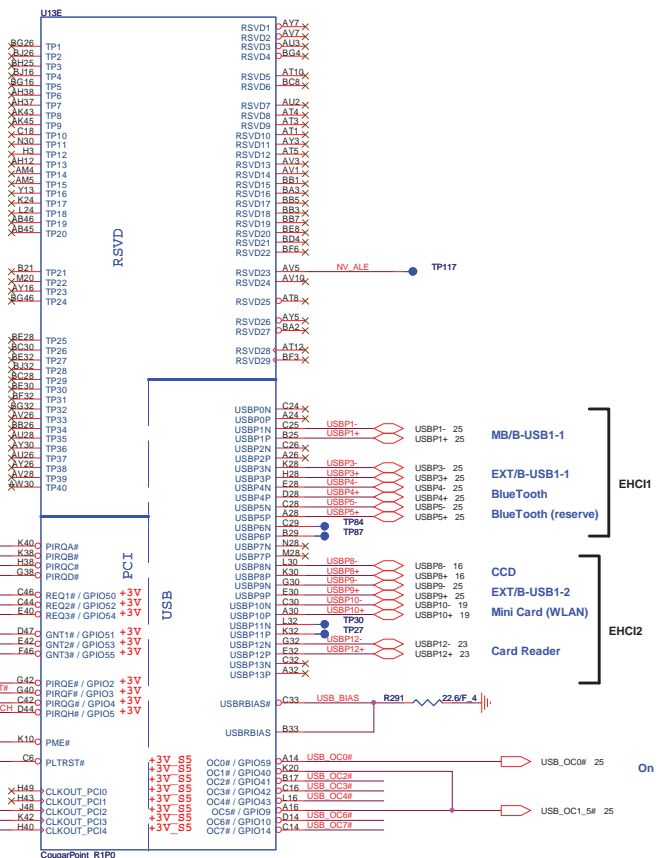
System PWR_OK(CLG)



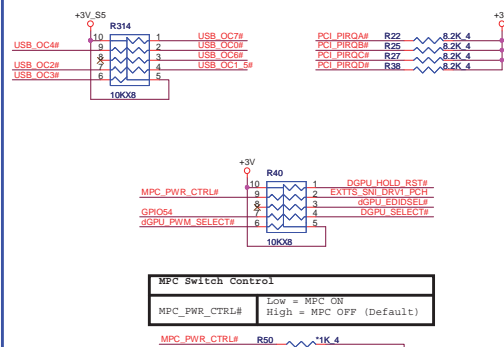
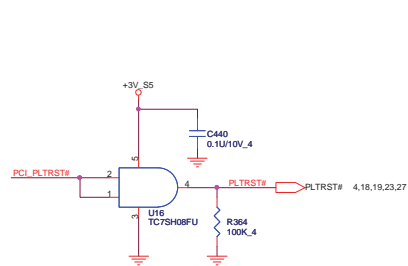
<http://hobi-elektronika.net>



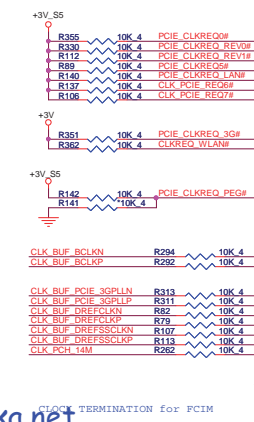
09

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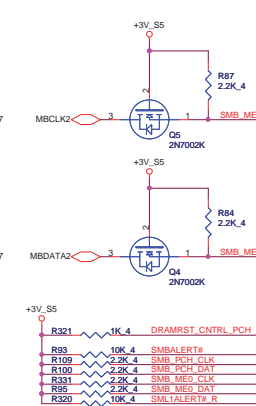
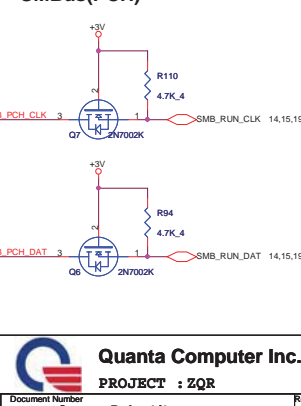
PCI/USBOC# Pull-up(CLG)



CLK_REQ/Strap Pin(CLG)



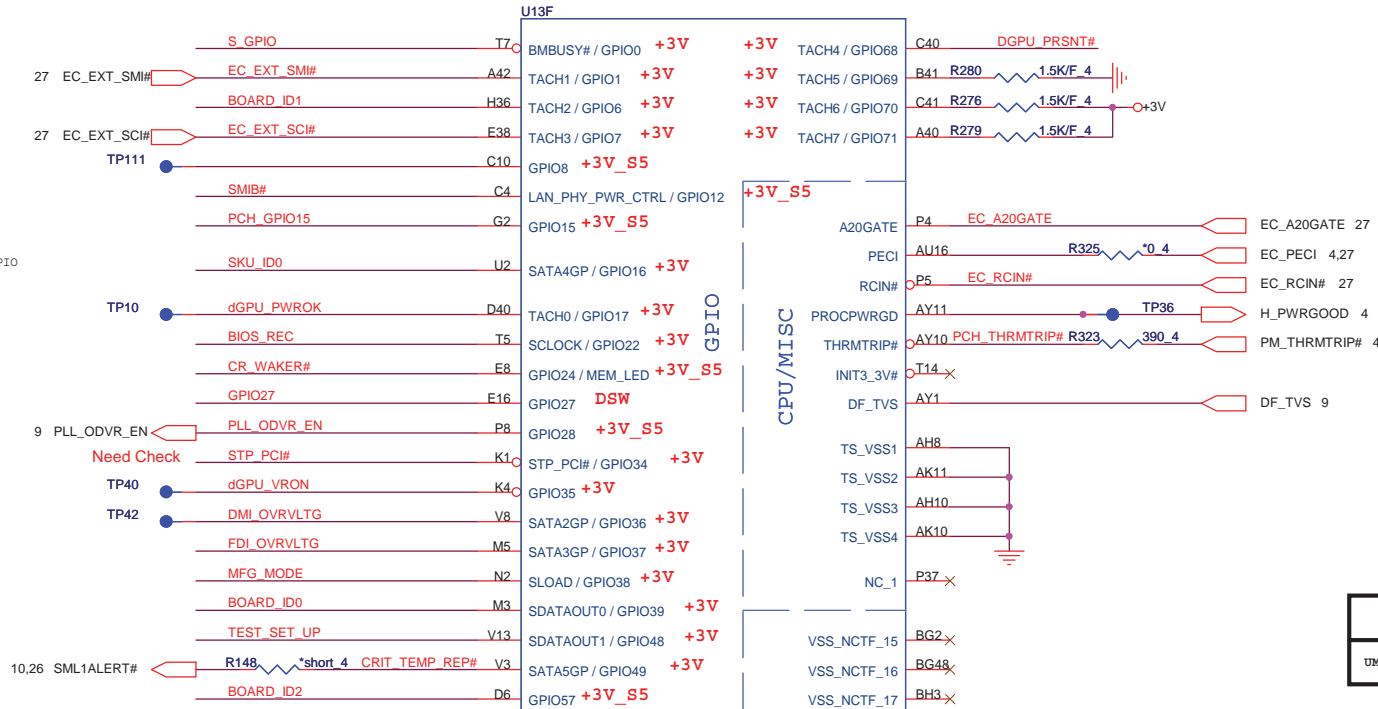
SMBus/Pull-up(CLG)

**SMBus(PCH)**

Cougar Point (GPIO,VSS_NCTF,RSVD)

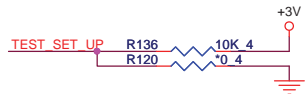
11

check VR_ON GPIO



| | DGPU_PRSENT# (GPIO68) | SKU_ID1 (GPIO64) | SKU_ID0 (GPIO16) | VGA H/W Signal | Setup Menu | |
|----------|--------------------------|---------------------|---------------------|-------------------|---------------|----------|
| UMA Only | 1 | 0 | 0 | UMA | Hidden | UMA boot |

SV_SET_UP
High = Strong (Default)



Intel ME Crypto Transport Layer
Security (TLS) cipher suite
Low = Disable (Default)
High = Enable

SGPIO



MFG-TEST

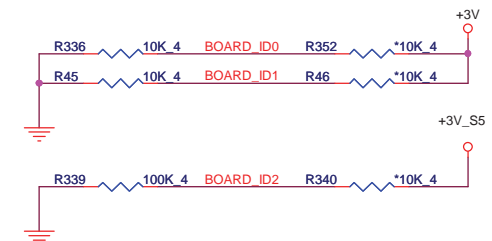
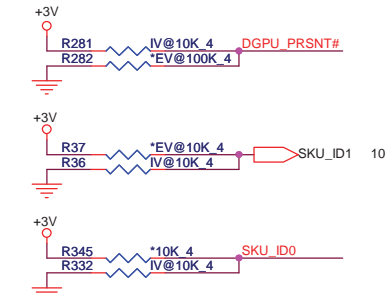
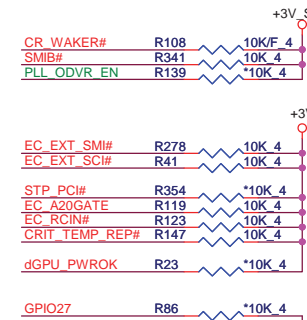


FDI TERMINATION
VOLTAGE OVERRIDE
Low - Tx, Rx terminated
to same voltage

DMI TERMINATION
VOLTAGE OVERRIDE
Low = Tx, Rx terminated to
same voltage (DC Coupling Mode)
(DEFAULT)

BIOS RECOVERY
High = Disable (Default)
Low = Enable

GPIO Pull-up/Pull-down(CLG)

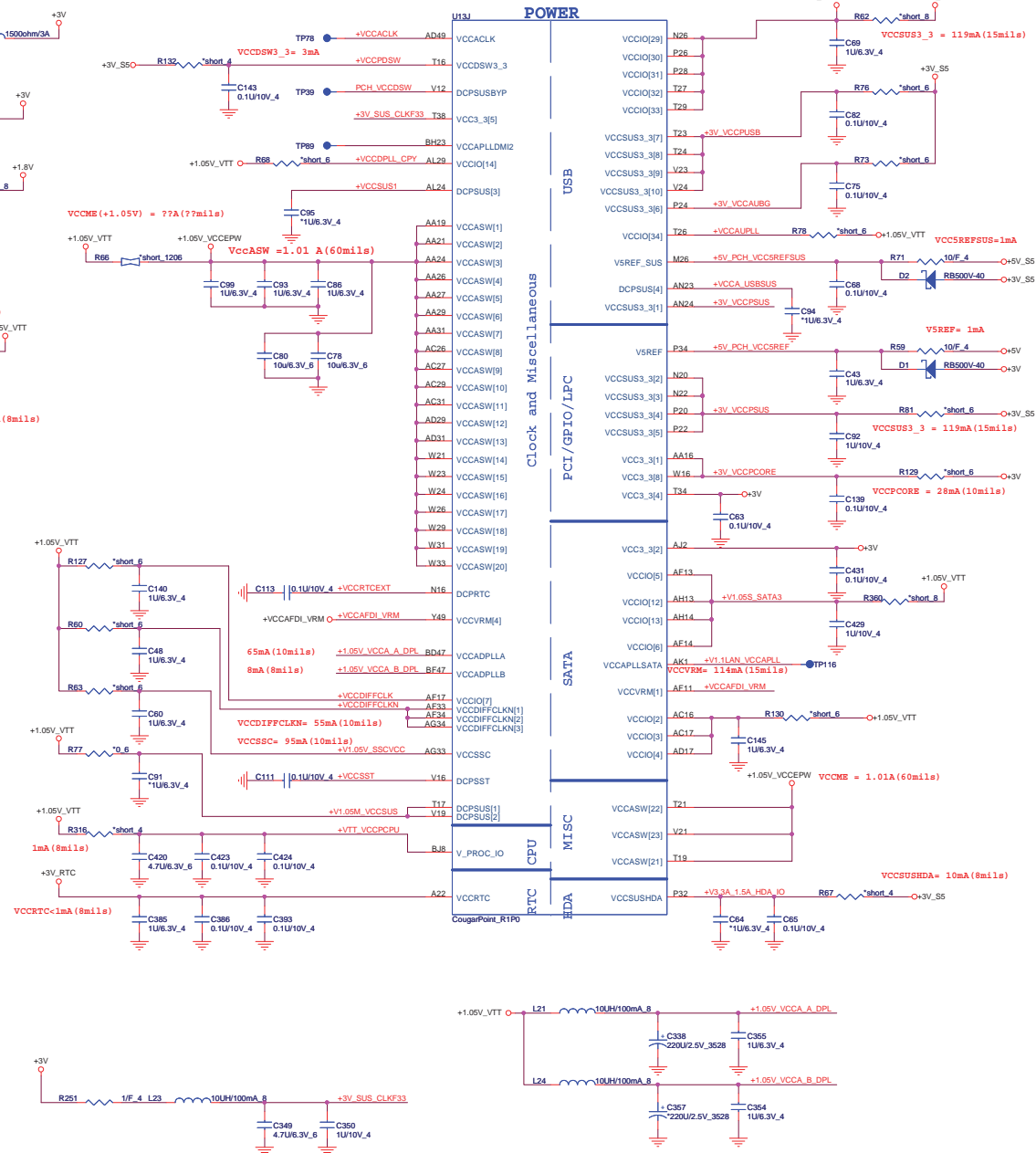


Quanta Computer Inc.
PROJECT : ZQR

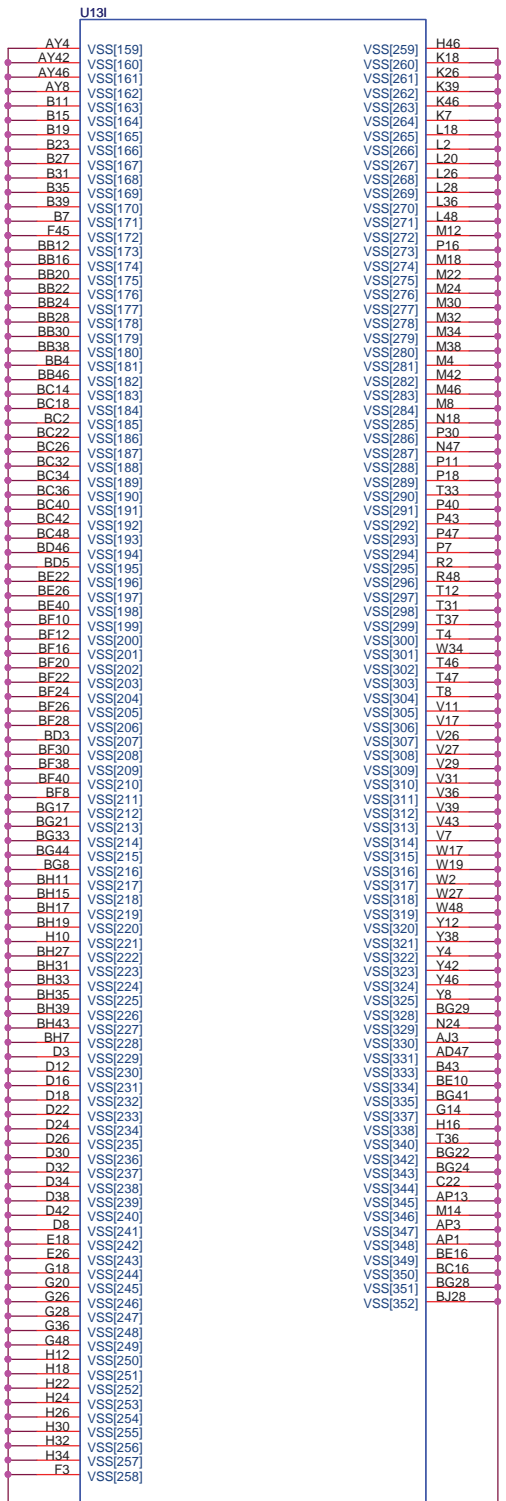
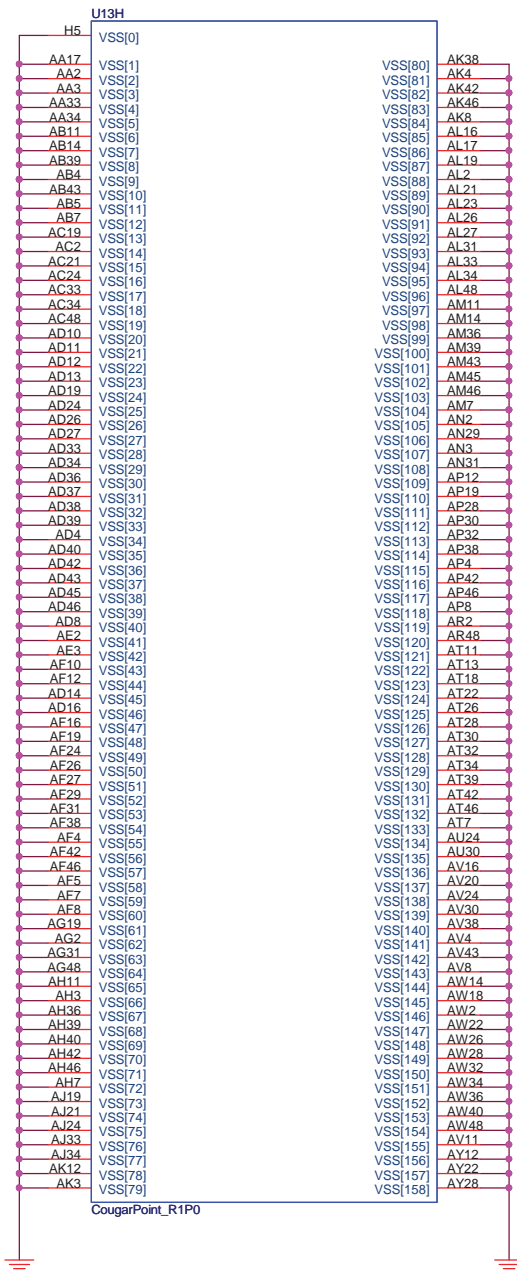
| | | |
|-------------------------|-----------------|--------|
| Size | Document Number | Rev 1A |
| Cougar Point 4/6 | | |

Date: Monday, May 23, 2011 Sheet 11 of 35

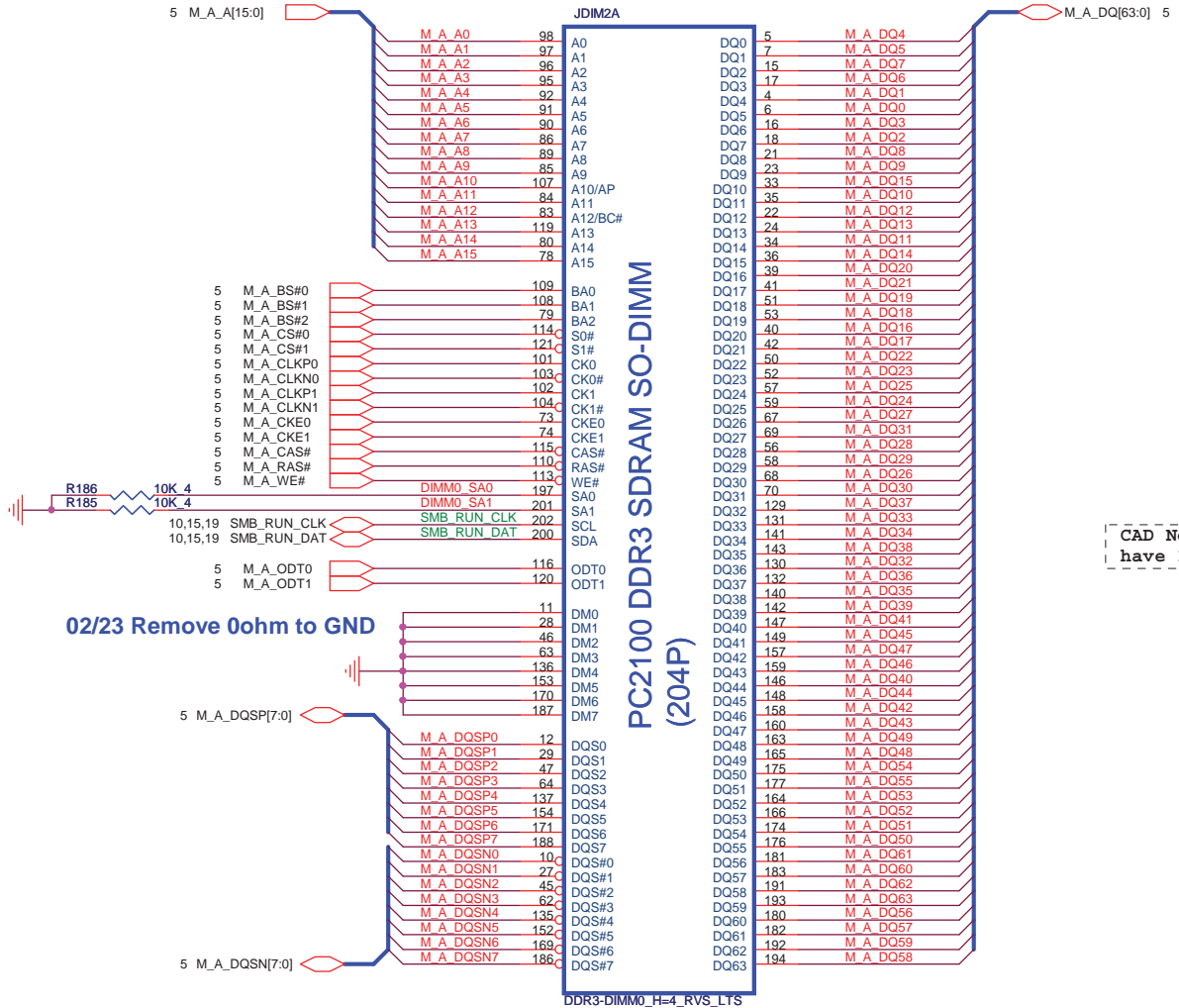
Cougar Point-M (POWER)



IBEX PEAK-M (GND)



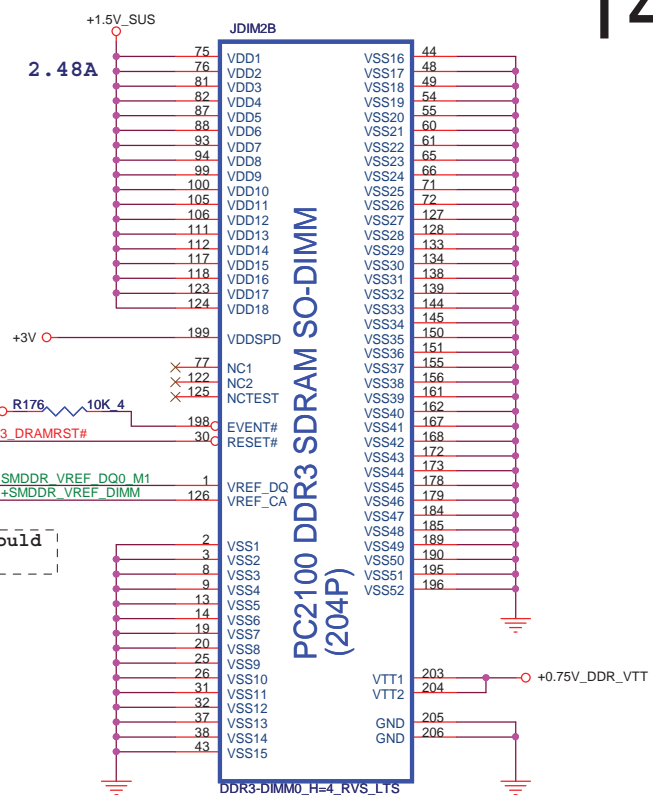
DDR RVS 4H



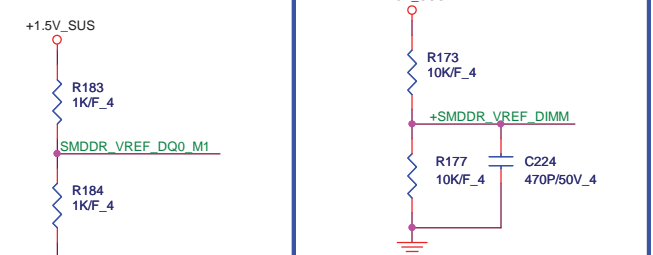
02/23 Remove 0ohm to GND

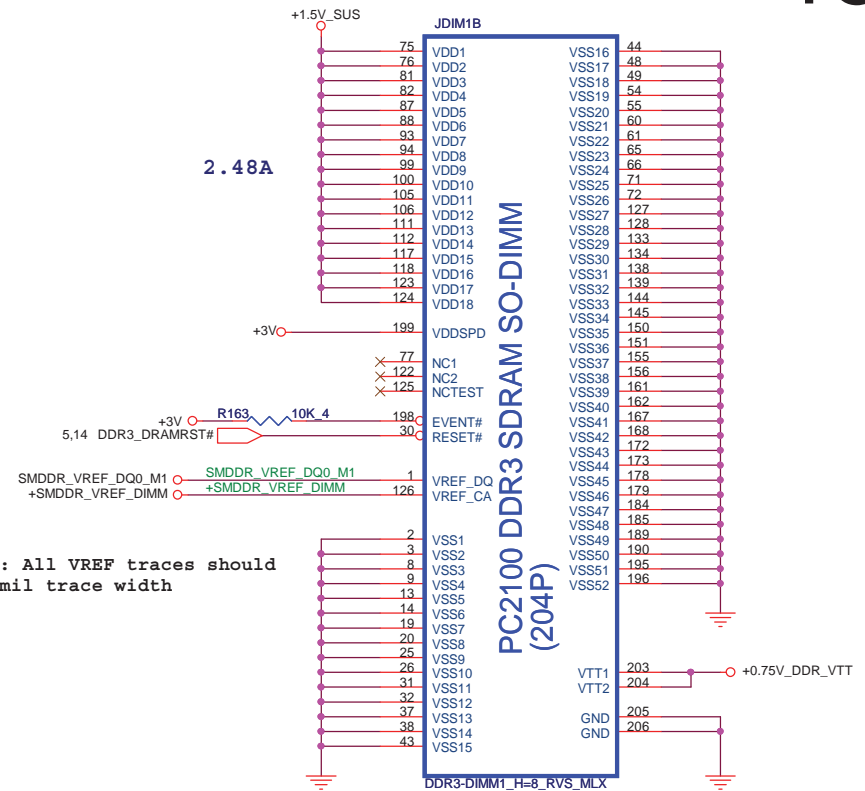
Place these Caps near So-Dimm0.

CAD Note: All VREF traces should have 10 mil trace width



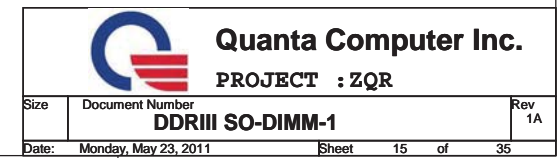
VREF DQ0 M1 Solution





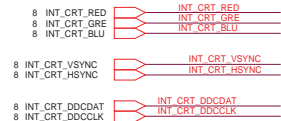
PC2100 DDR3 SDRAM SO-DIMM
(204P)

DDR3-DIMM1_H=8_RVS_MLX

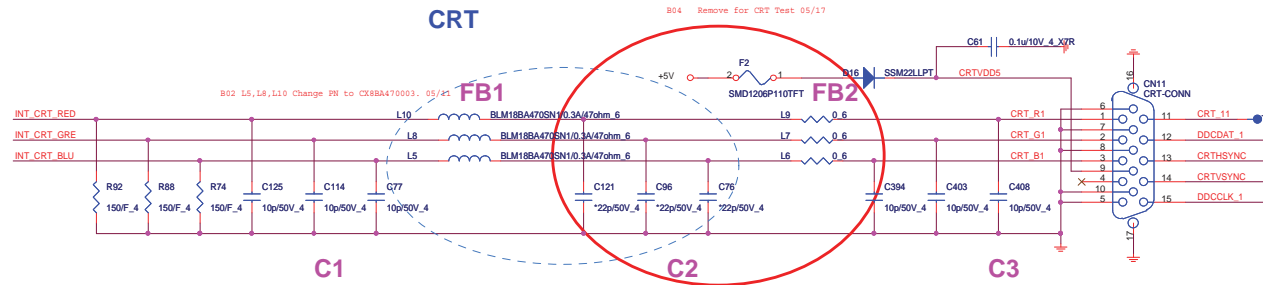


CRT Switch

0_ohm Resistor place close to Joint-Point



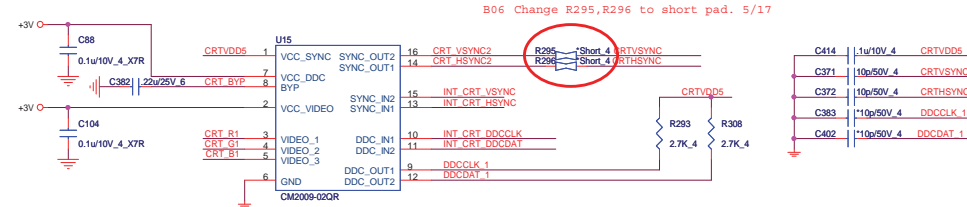
CRT



Note: this video filter is a 2-pole, low-pass filter configuration with a target design cutoff frequency of ~200MHZ

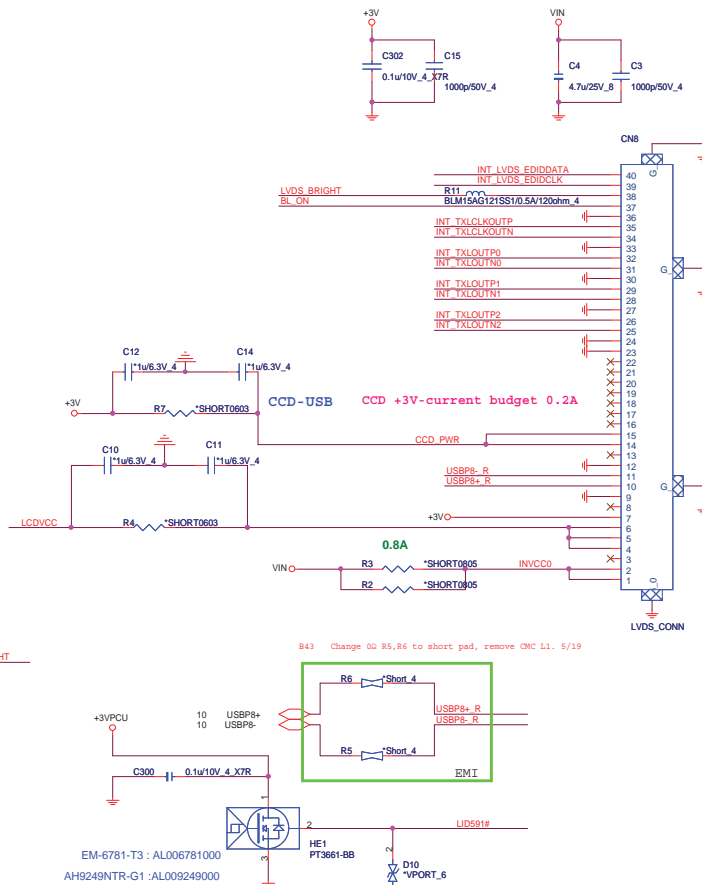
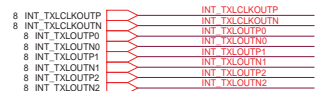
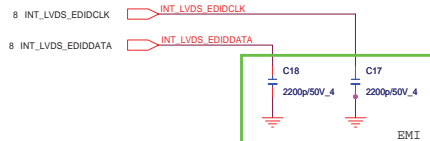
C1: 10pF, C2: 22pF, C3: 10pF,

FB1: 47ohm@100MHZ, FB2: 47ohm@100MHZ

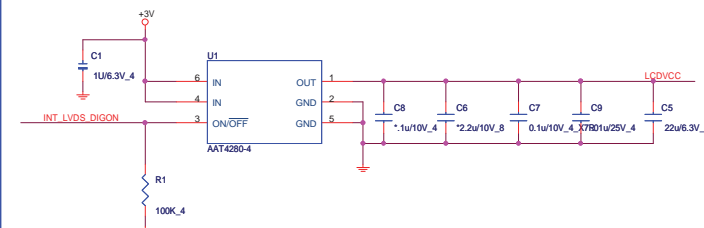


LVDS

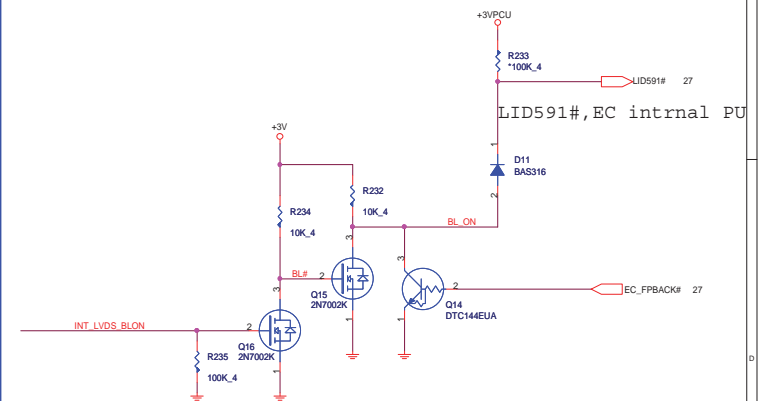
0_ohm Resistor place close to Joint-Point



LCD Power

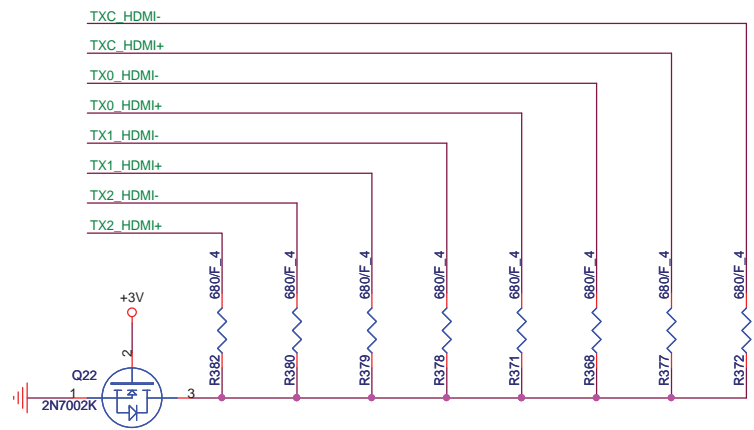


Backlight Control



Lid Switch (Hall sensor)

<http://hobi-elektronika.net>

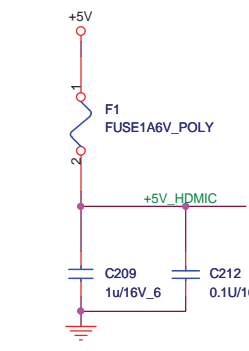
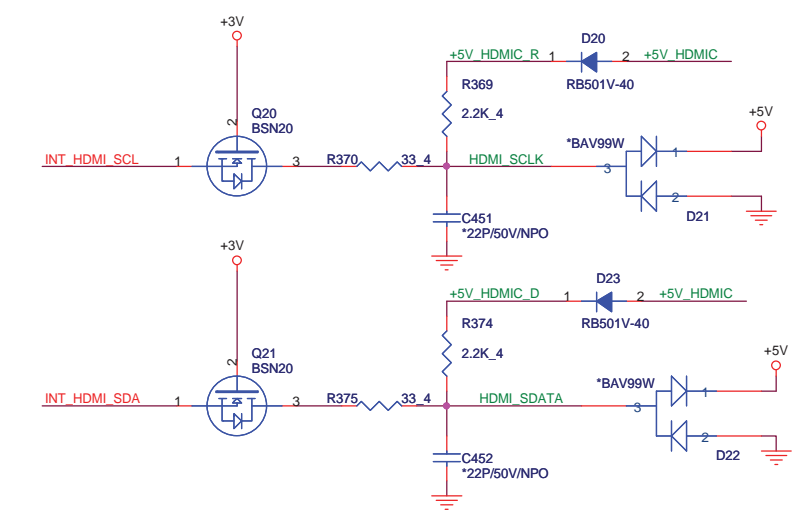
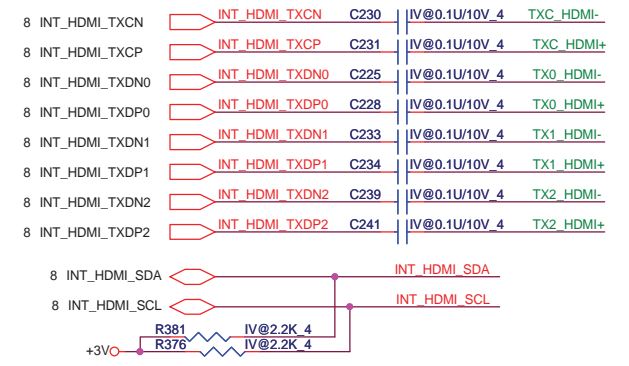


| | EV@ | IV@ |
|-----|---------|---------|
| SP@ | 500 ohm | 680 ohm |

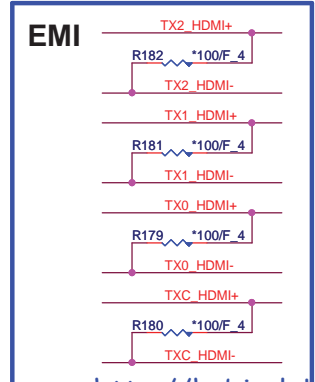
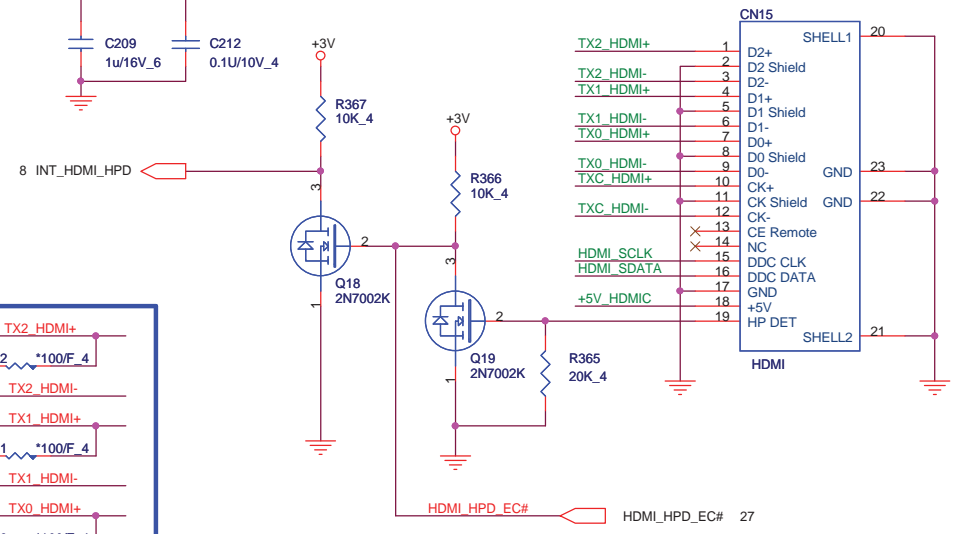
PLACE PULL DOWN RESISTORS CLOSE TO DIFFERENTIAL PAIRS CONNECTED TO SOLID GROUND FLOOD WHICH IS CONTROLLED BY THE FET
AVOID STUBS TO ALL DIFFERENTIAL TRACES

INT-HDMI

PLACE AC CAP
CLOSE TO CONNECTOR



HDMI CONN



```
<BOM note>
If center tap power come from internal switch
regulator
=>Stuff 52SWR@ (Default)
If center tap power come from internal LDO
=>Stuff 52LDO@
```



B27 L11 change from 0 Ω to short pad. 5/18

VDDCT

CX82EG60100

L11

0.5A/600mOhm

100k

C158

1uF/6.3V

AVDD_CEN

C174

0.1uF/16V

C177

1000pF/50V

C162

0.1uF/16V

C169

1000pF/50V

TX1N

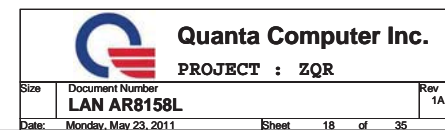
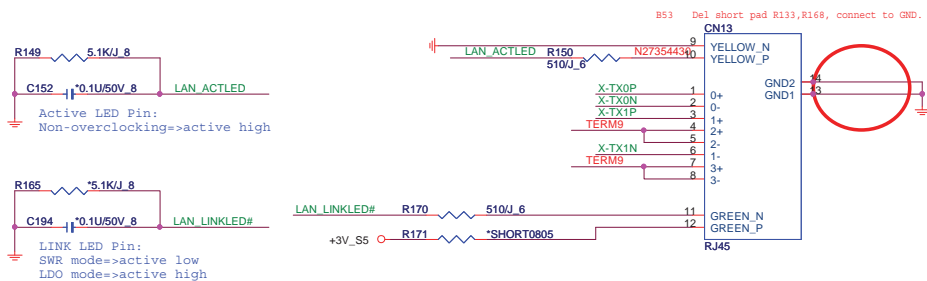
TX1P

TXN

TXOP

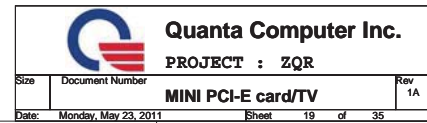
D3: CY003100Z06 (2nd) / CY231T20Z00 (1st & non prefer)

U17,U18: BC0251T2Z00 (2nd) / BC0251T2Z00 (1st)

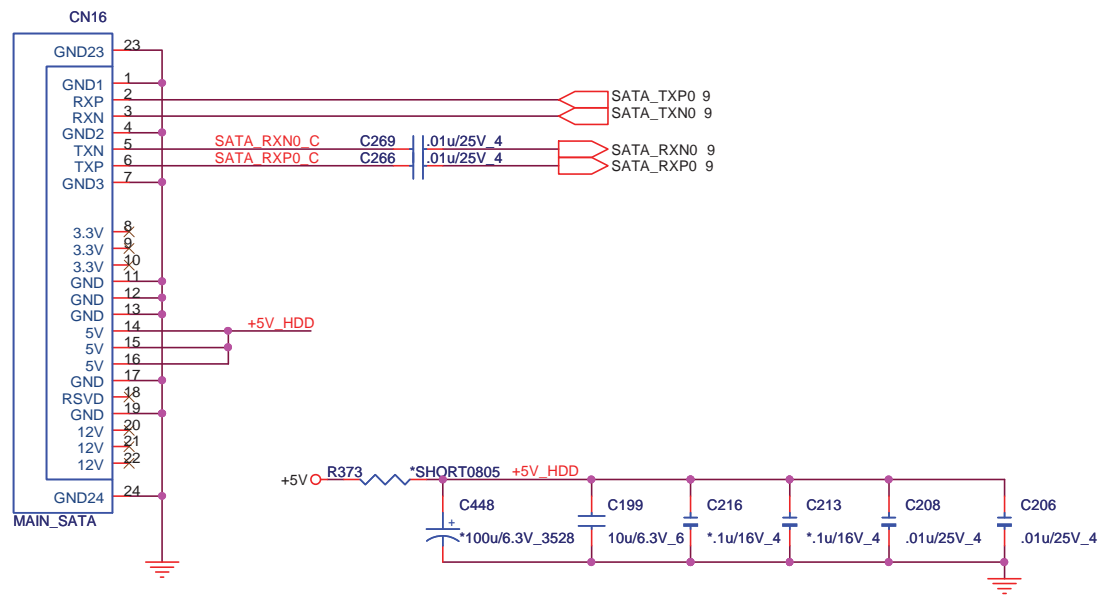


+3.3V: 1000mA
+3.3Vaux:330mA
+1.5V:500mA

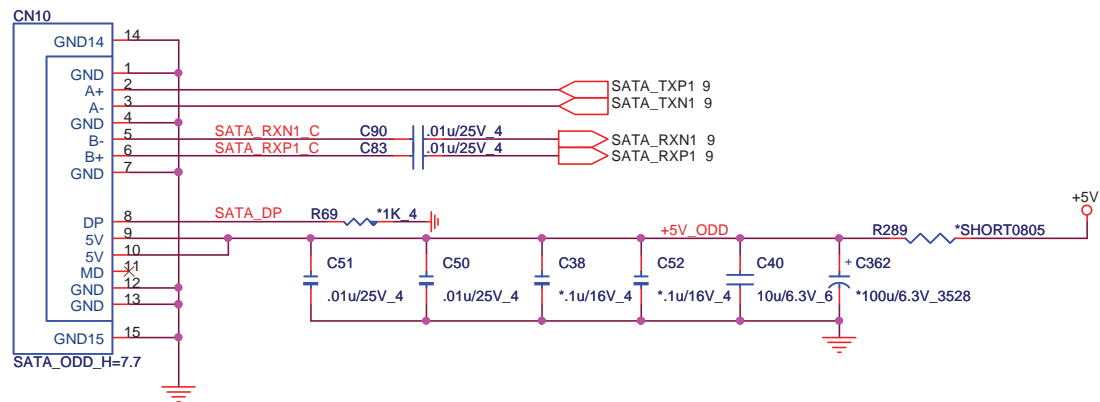
H=7.0mm
LTS_AAA-PCI-046-K01



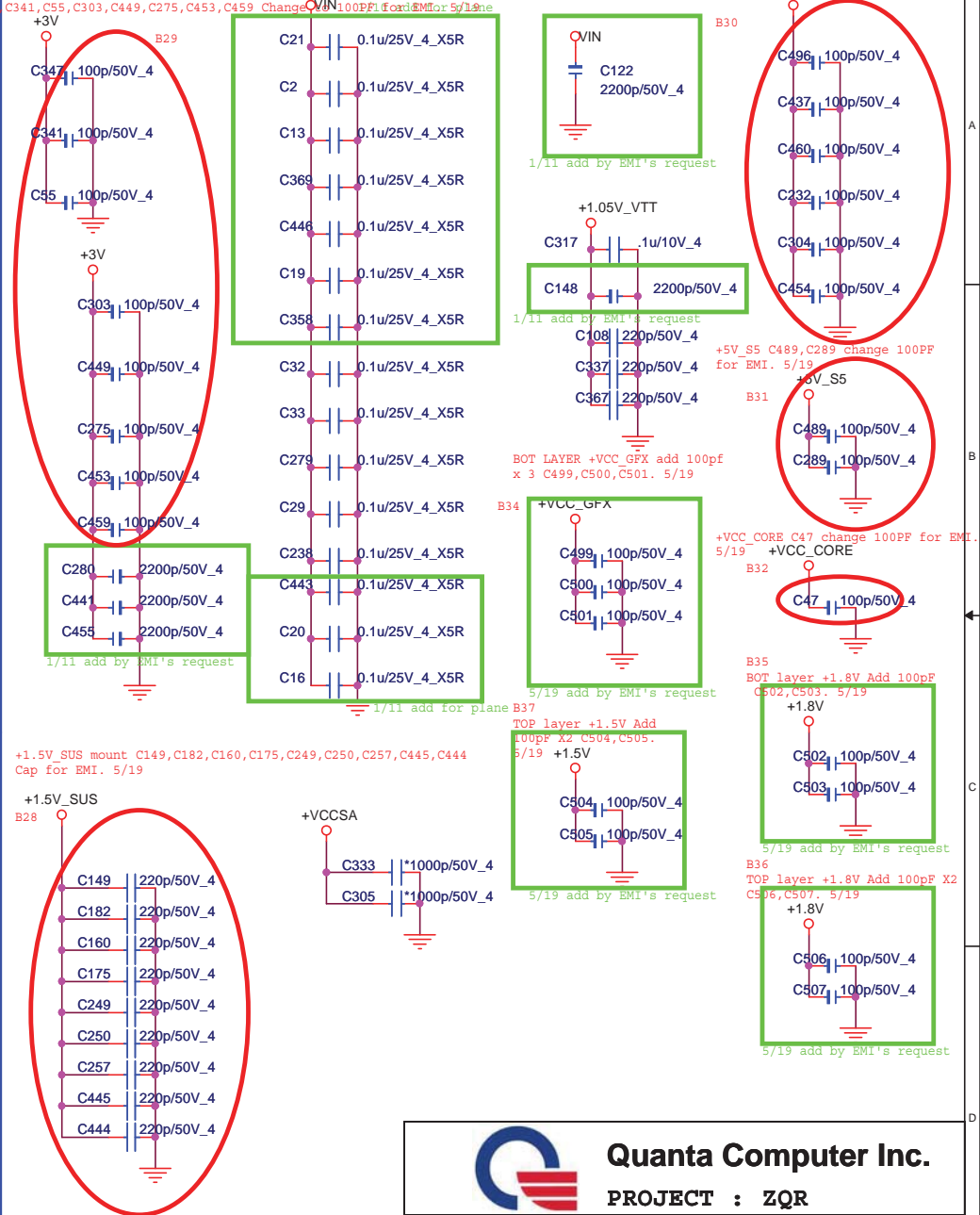
MAIN SATA HDD



ODD (SATA)



EE RETURN-PATH CAPACITORS



Codec(ADO)



HP

22 HP-L

23 HP-R

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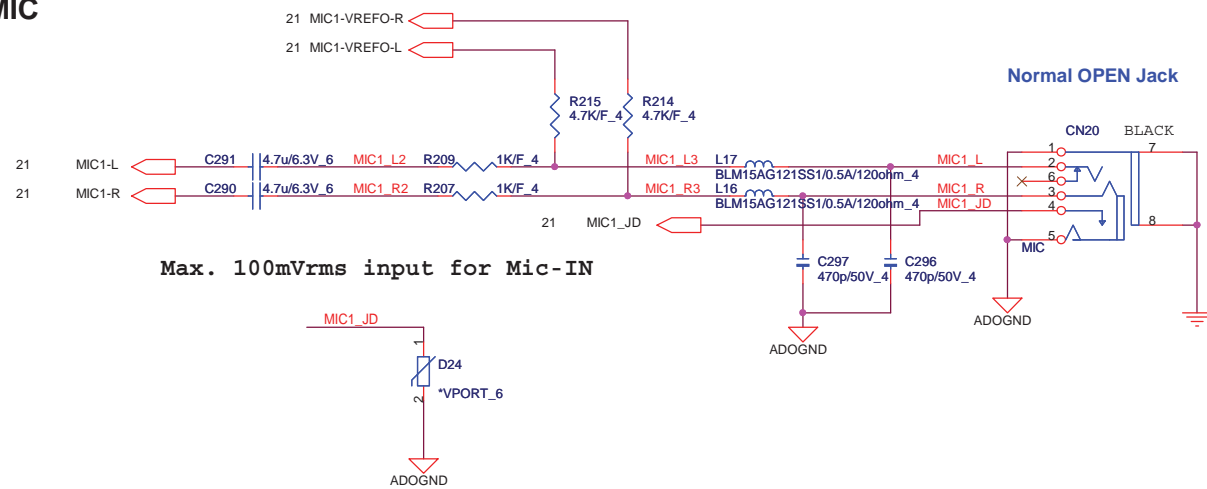
62

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64

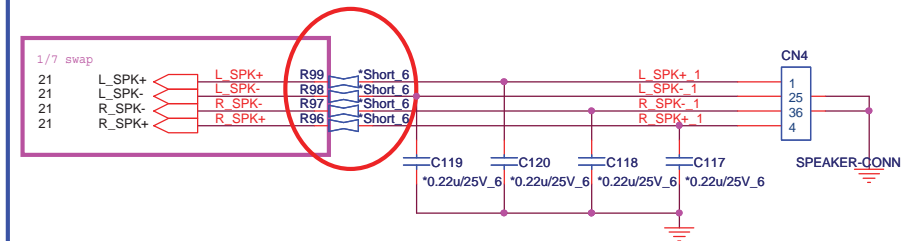
65

MIC

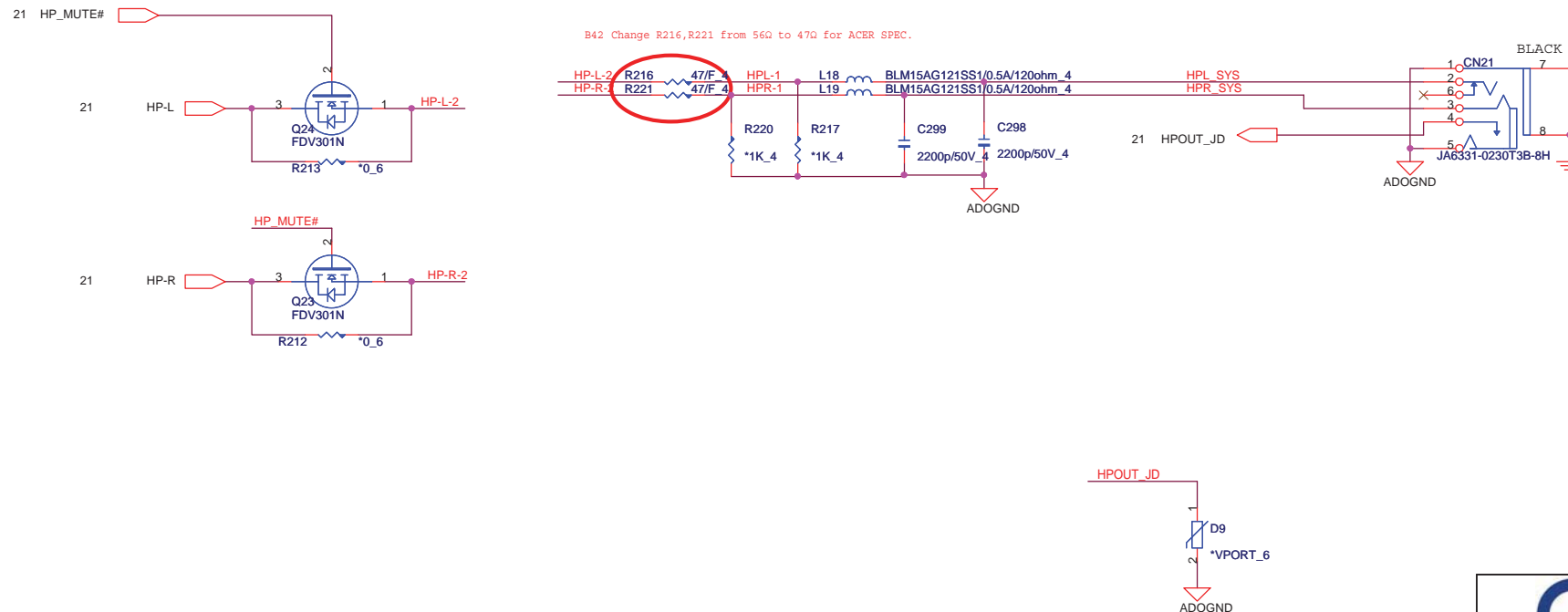


Internal Speaker

B27 R96,R97,R98,R99 change from 0 Ω to short pad. 5/18



HP/SPDIF

**Quanta Computer Inc.**

PROJECT : ZQR

AMP /AUDIO JACK CONN

| Size | Document Number |
|------|-----------------|
|------|-----------------|

Date: Monday, May 23, 2011

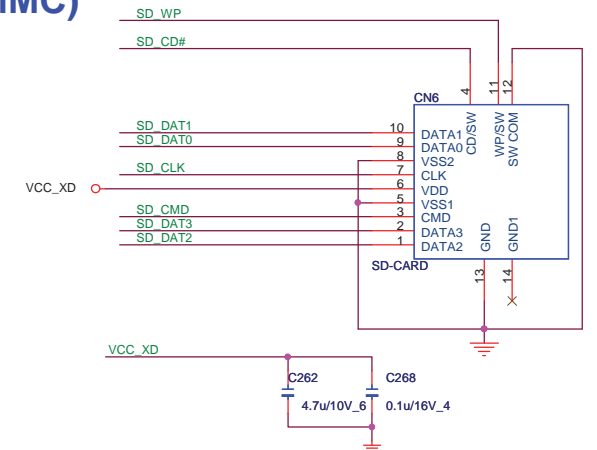
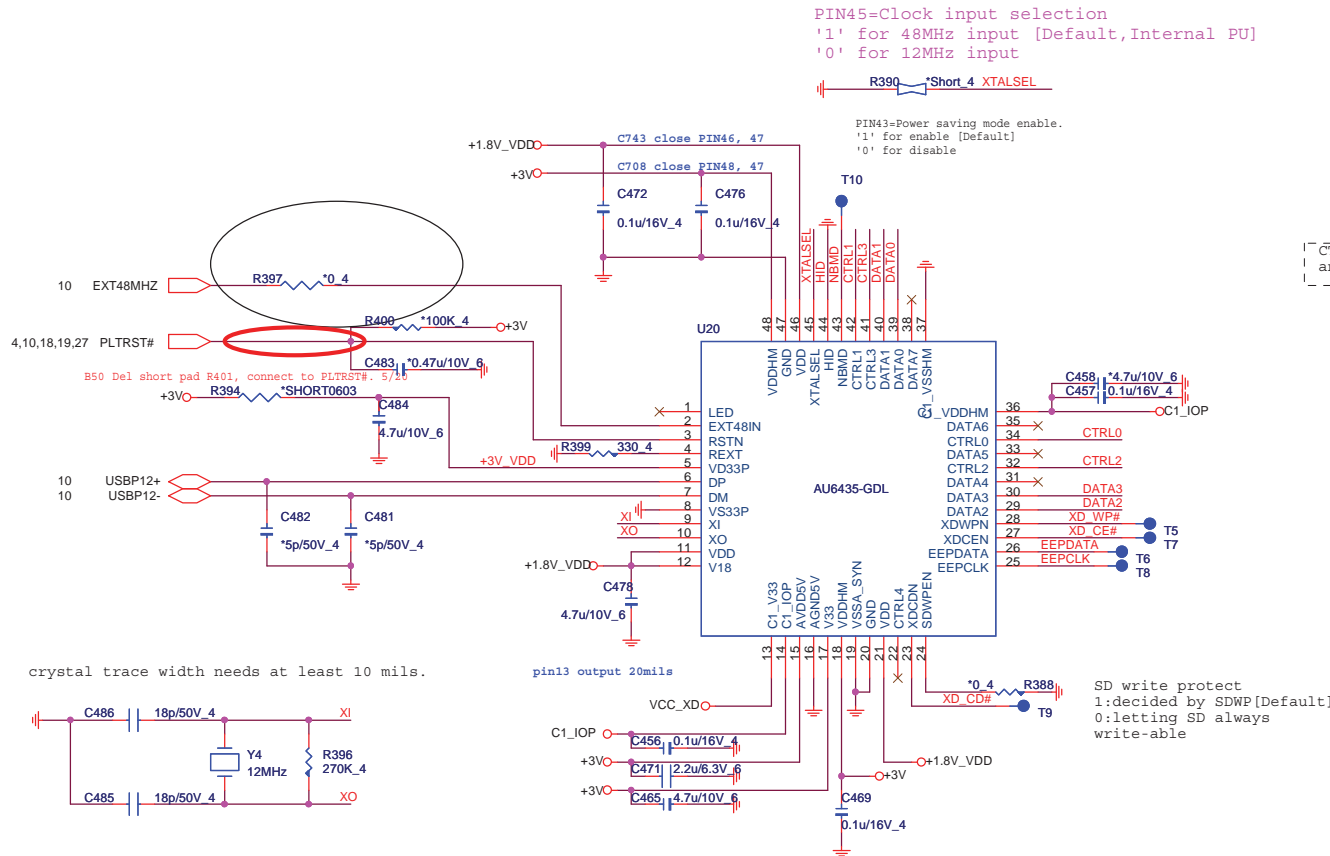
Sheet 22 of 35

Rev
1A

CARD READER Controller AU6435-GDL

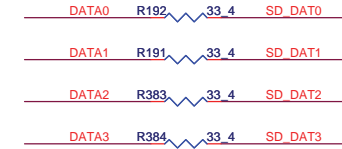
2 IN 1 CARD READER (SD/MMC)

| | |
|--------|-------------|
| Main | DFHS11FR011 |
| Second | DFHS11FR033 |

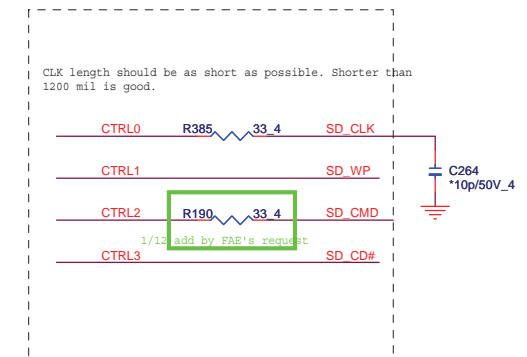


CTRL0, CTRL1 trace length shorter,
and surround with GND.

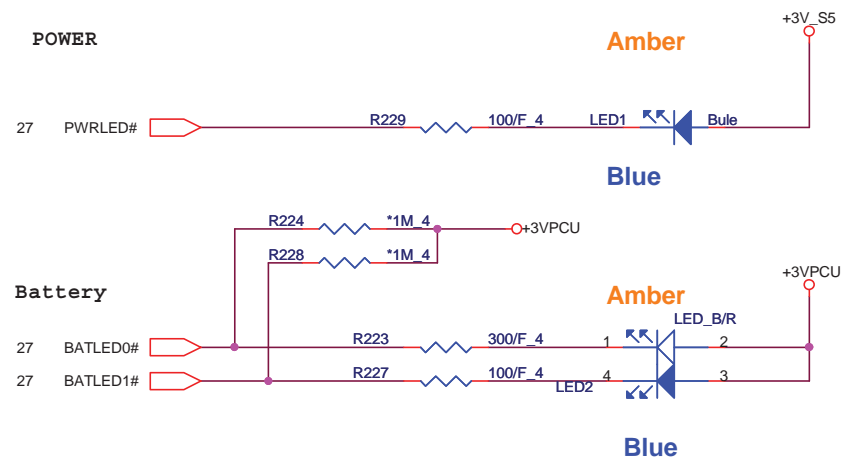
The trace length difference for each card interfaces should be smaller than 500 mil




Close to connector

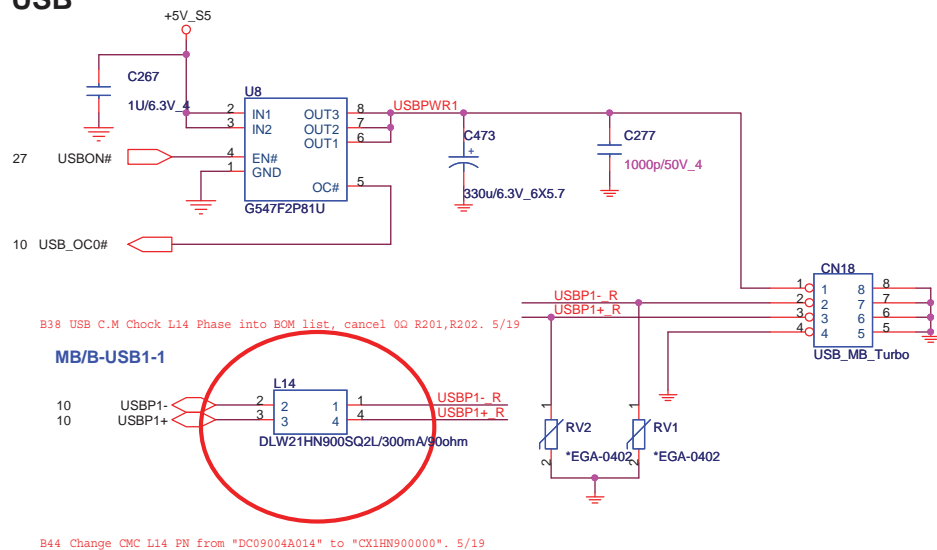


LED

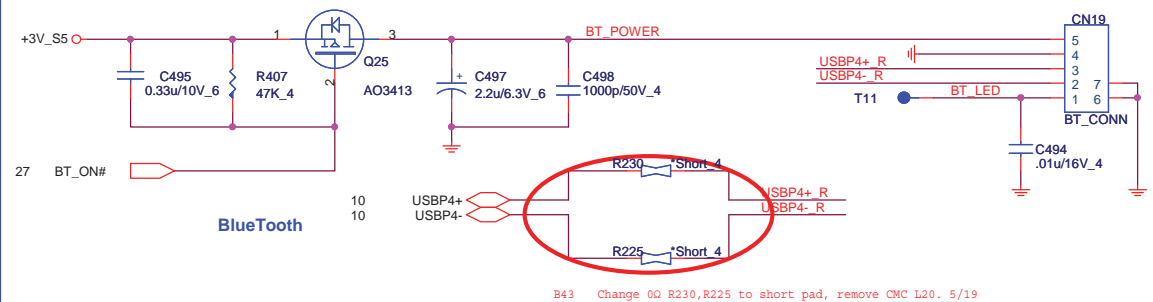


| | | |
|---|-----------------|-----------------------------|
|  Quanta Computer Inc. PROJECT : ZQR | | Rev 1A |
| | | POWER/MMB/LAUNCH/LED |
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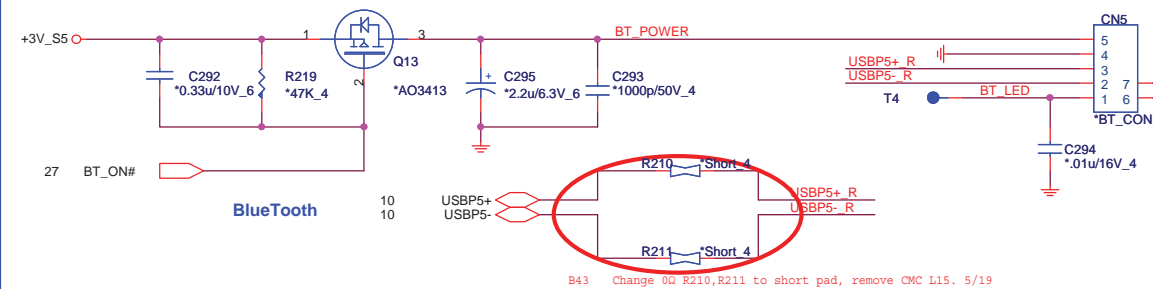
USB



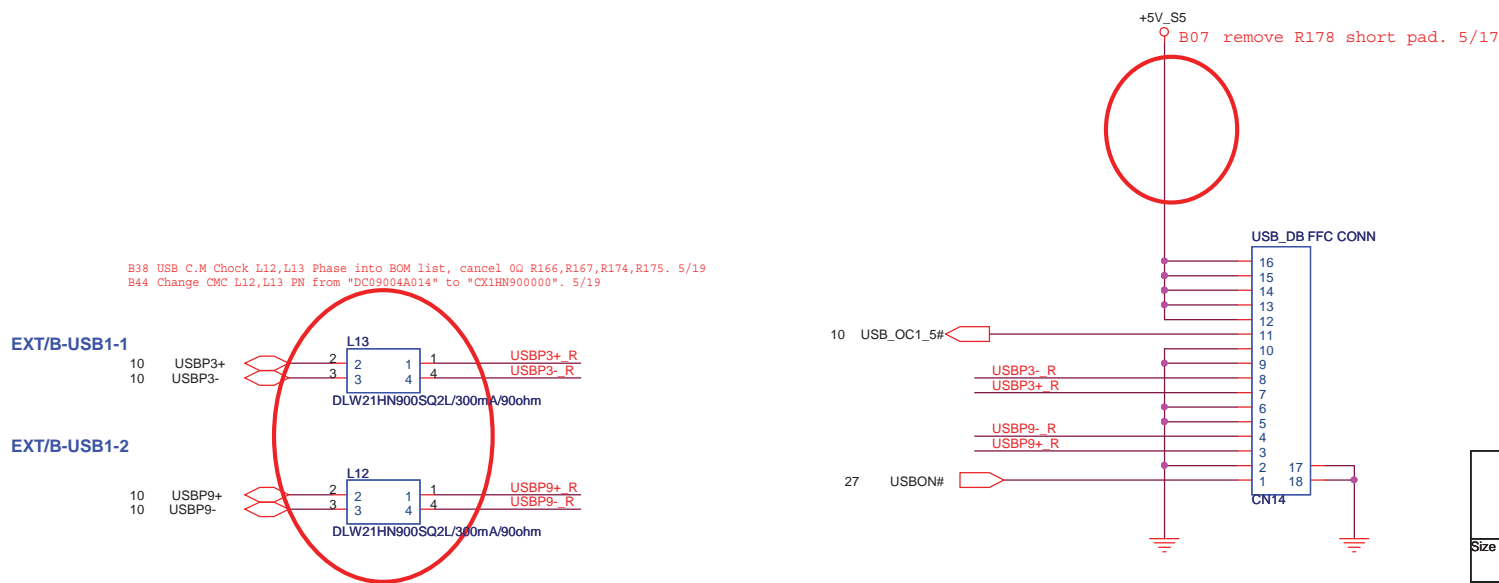
BLUETOOTH CONNECTOR for 3.0




Reserve



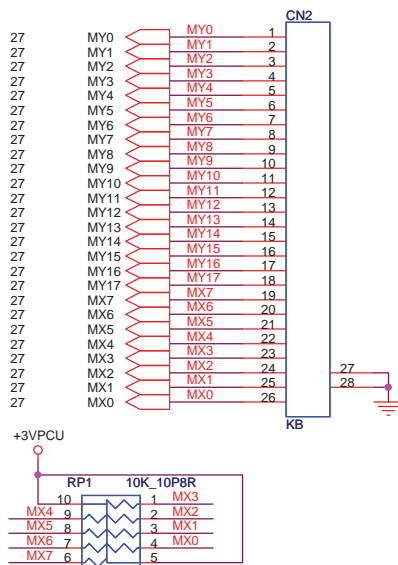
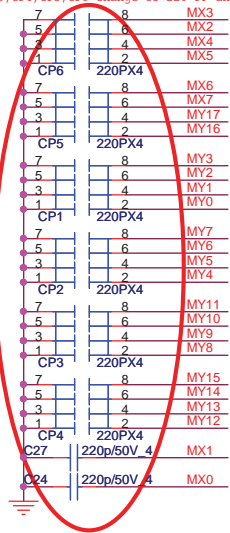
USB/B



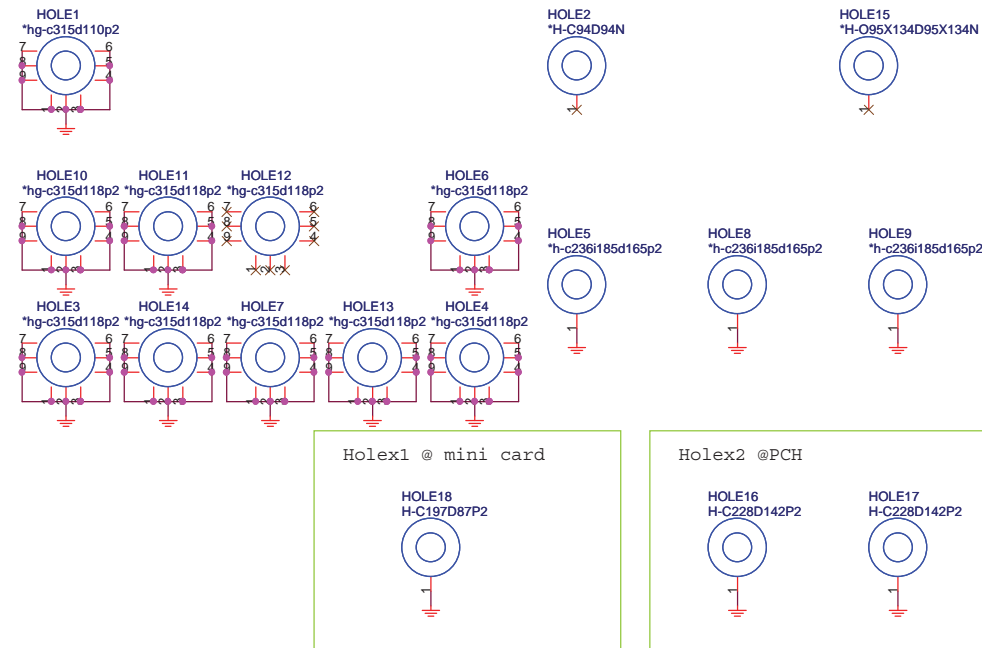
| | | |
|---|----------------------|----------------|
|  Quanta Computer Inc. PROJECT : ZQR | | Rev 1A |
| Size | Document Number | |
| USB/ BT | | |
| Date: | Monday, May 23, 2011 | Sheet 25 of 35 |

K/B

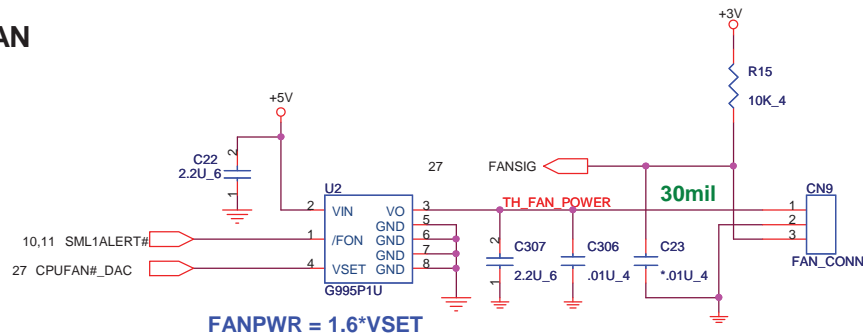
KB Cap CP1,CP2,CP3,CP4,CP5,CP6 change to 220 PF and phase into BOM list. 5/19 B33



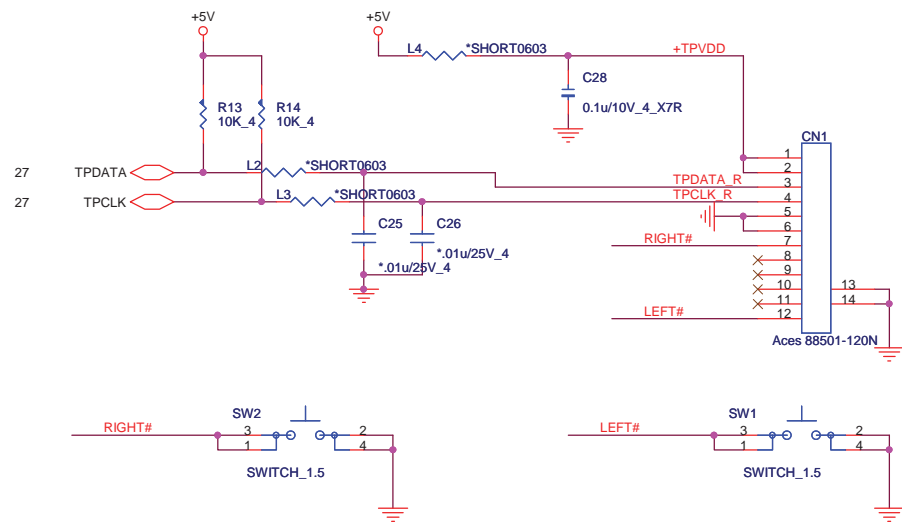
HOLE



CPU FAN



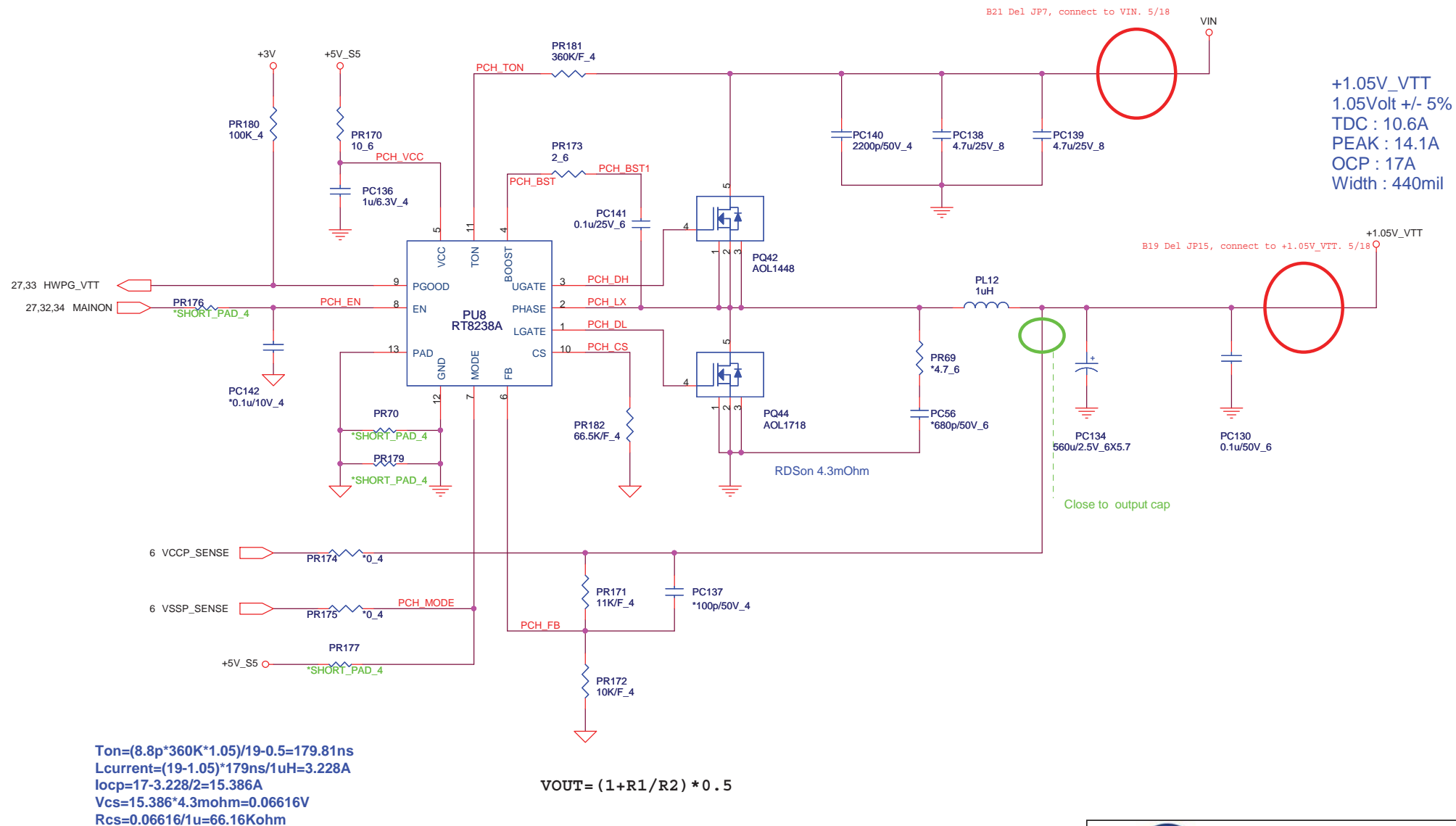
TOUCHPAD & Switch CONN.



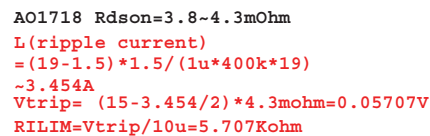
Quanta Computer Inc.
PROJECT : ZQR

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|------|-----------------|-----|
| | KB/FAN/TP+FP | 1A |

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+SMDDR_VREF
0.75 Volt +/- 5%
TDC : 0.38A
PEAK : 0.5A
Width : 20mil

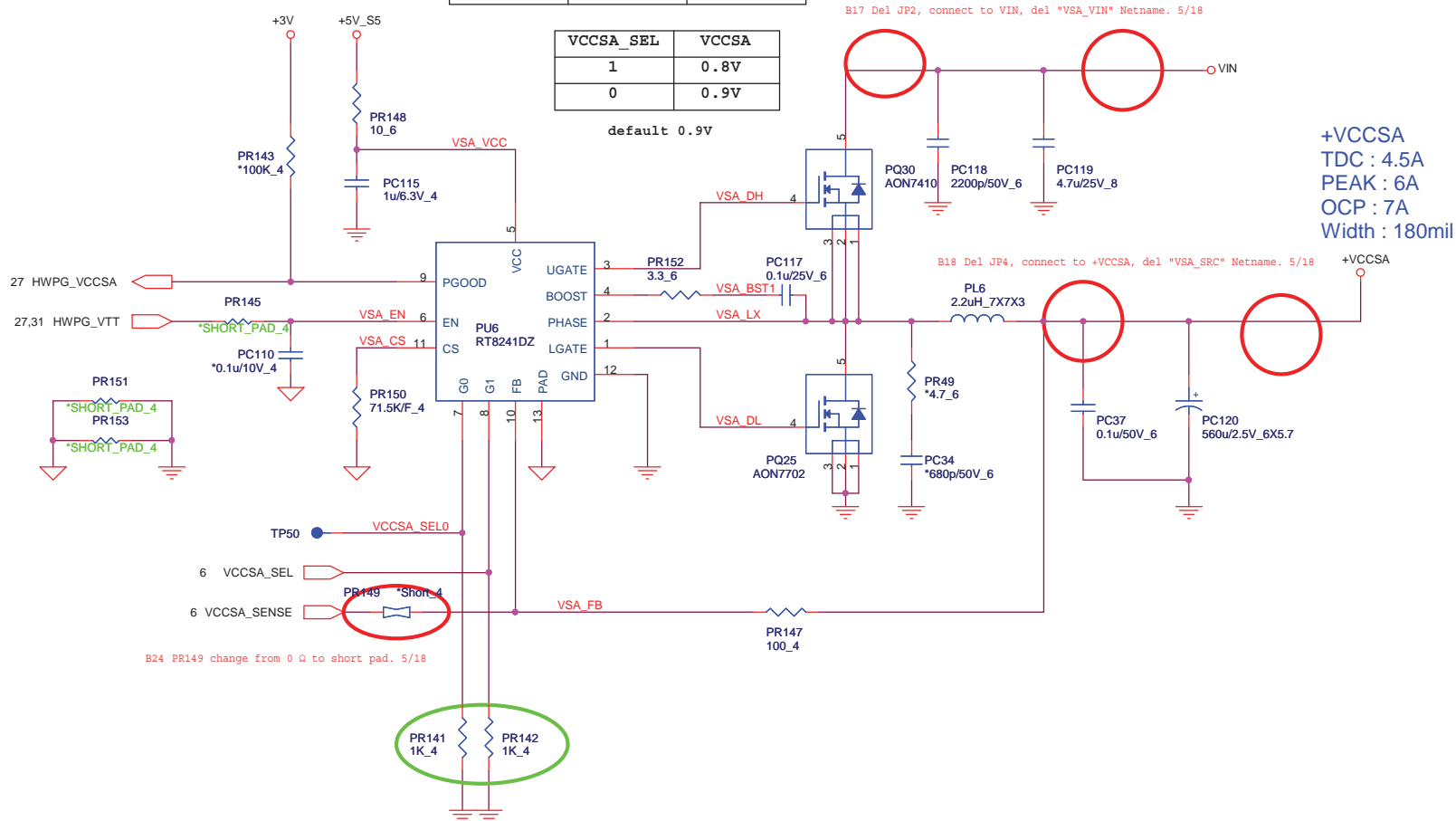


| | S3 | S5 | +1.5VSUS | REF | VTT |
|-------|----|----|----------|-----|-----|
| S0 | 1 | 1 | ON | ON | ON |
| S3 | 0 | 1 | ON | ON | OFF |
| S4/S5 | 0 | 0 | OFF | OFF | OFF |

| G0 | G1 | VCCSA |
|----|----|--------|
| 0 | 0 | 0.9V |
| 0 | 1 | 0.8V |
| 1 | 0 | 0.725V |
| 1 | 1 | 0.675V |

| VCCSA_SEL | VCCSA |
|-----------|-------|
| 1 | 0.8V |
| 0 | 0.9V |

default 0.9V




OCP=7A
 $I_{ripple} = (19 - 0.9) * 0.9 / (2.2u * 300K * 19)$
 $= 1.299A$
 $R_{th} = 14mohm * 8 * (7 - 0.65) / 10uA$
 $= 71.125K$
 $I_{peak} = 8.299A$



Quanta Computer Inc.
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| Size | Document Number | Rev |
|-------|----------------------|----------------|
| | +VCCSA(RT8241A) | 1A |
| Date: | Monday, May 23, 2011 | Sheet 33 of 35 |

| | | | | |
|---------------------|-----|--|--|--|
| Model ZQR MB | REV | CHANGE LIST | | |
| | B | <p>2011/05/11</p> <p>B01 remove PR22 from BOM for power up issue. B02 L5,L8,L10 Change PN to CX8BA470003.</p> <p>2011/05/16</p> <p>B03 Change net closed to Audio Codec PCBEEP netname to BEEP_2</p> <p>2011/05/17</p> <p>B04 Change L6,L7,L9 to 0Ω, remove C76,C96,C121 for CRT Test. B05 Add R409, remove U5, C142 for saving cost. B06 Change Bottom side 0Ω to short pad for cost and SMT cycle time issue; R284,R295,R296,R392,R395,R401,R402,R403,R404,R408. B07 Remove R178 short pad, connect to +5V_S5. B08 Change "+VIN_VCC_CORE" net to Vin. B09 Del JP1,JP13, connect to Vin, del "+VIN_VCC_CORE" netname. B10 Del JP3, connect to Vin. Del "VCC_GT_VIN" netname. B11 Del JP9,JP10 connect to Vin. B12 Del JP11, connect to +3VPCU. B13 Del JP12, connect to +5VPCU. B14 PQ23 ~ PQ24 change symbol from N-MOS to P-MOS</p> <p>2011/05/18</p> <p>B15 Del JP14, connect to +1.8V. B16 Del JP6, connect to +3VPCU. B17 Del JP2, connect to VIN, del "VSA_VIN" Netname. B18 Del JP4, connect to +VCCSA, del "VSA_SRC" Netname. B19 Del JP15, connect to +1.05V_VTT. B20 Del JP5, connect to +1.5VSUS, del "+1.5VSUS_SRC" Netname. B21 Del JP7,JP8 connect to VIN. B22 Change "+1.5VSUS_SRC" Netname to "+1.5V_SUS". B23 Mount C70, C71 for +Vcc_core overshoot issue. B24 PR29,PR30,PR35,PR37,PR41,PR46,PR93,PR120,PR128,PR132,PR149(0_4) change from 0ohm to short-pad. B25 PR178(0_6) change from 0ohm to short-pad. B26 R114,R197,R206(0_4) change from 0ohm to short-pad. B27 L11,PR64,PR73,PR75,R96,R97,R98,R99,R133,R168(0_6) change from 0ohm to short-pad.</p> <p>2011/05/19</p> <p>B28 Page 20 +1.5V_SUS mount C149,C182,C160,C175,C249,C250,C257,C445,C444 Cap for EMI B29 Page 20 +3V C347,C341,C55,C303,C449,C275,C453,C459 Change to 100PF for EMI. B30 Page 20 +5V C496,C437,C460,C232,C304,C454 change 100PF for EMI. B31 Page 20 +5V_S5 C489,C289 change 100PF for EMI. B32 Page 20 +VCC_CORE C47 change 100PF for EMI. B33 KB Cap CP1,CP2,CP3,CP4,CP5,CP6 change to 220 PF and phase into BOM list for EMI. B34 BOT layer +VCC_GFX add 100pf x 3 C499,C500,C501 for EMI. B35 BOT layer +1.8V Add 100pF X2 C502,C503 for EMI. B36 TOP layer +1.8V Add 100pF X2 C506,C507 for EMI. B37 TOP layer +1.5V Add 100pF X2 C504,C505 for EMI. B38 USB C.M Chock L12,L13,L14 Phase into BOM list, cancel 0Ω R166,R167,R174,R175,R201,R202 for EMI. B39 PR4 4.7ohm / PC5 1000pf phase into BOM list for EMI. B40 Change R286 from 220 to short pad. B41 Add a MOSFET Q26,R410,R412 to separate CODE SYNC and PCH Strap signal to avoid leakage issue. B42 Change R216,R221 from 56Ω to 47Ω for ACER SPEC. B43 Change 0Ω R5,R6,R210,R211,R225,R230 to short pad, remove CMC L1,L15,L20 for SMT. B44 Change CMC L12,L13,L14 PN from "DC09004A014" to "CX1HN900000". B45 Remove C315 for cost issue.</p> <p>2011/05/20</p> <p>B46 R392,R197 change from short pad to 0Ω. B47 Del short pad R114, connect to PCIE_CLKREQ_LAN#. B48 Del short pad R206, connect to MIC1-VREF0-L. B49 Del short pad R264, connect to HP_VB#. B50 Del short pad R401, connect to PLTRST#. B51 Del short pad R403, connect to HP_MUTE#. B52 Del short pad R386, del netname ACZ_SDIN0_R, connect to ACZ_SDIN0. B53 Del short pad R133,R168, connect to GND. B54 Del C442.</p> <p>2011/05/23</p> <p>B55 PR139 changes from 1.33Kohm(CS21332FB11) to 1.58Kohm(CS21582FB00). B56 PR130 changes from 2.55Kohm(CS22552FB01) to 2.49Kohm(CS22492BB00). B57 PC99 ~ PC103 change from 33nf(CH3334K1B00) to 0.1uf(CH4104K9B03).</p> | | |
| | | | | |
| 3C | | | | |

| | | | | | |
|--|--|-----------------|-----|------------------|--|
|  Quanta Computer Inc. | | PROJECT : ZQR | | DATE: 2011/05/09 | |
| DOC NO. | | PROJECT MODEL : | ZQR | APPROVED BY: | |
| Change list | | PART NUMBER: | | DRAWING BY: | |
| REV 1A | | REVISION: 1A | | | |
| Date: Monday, May 23, 2011 | | | | | |